2004

Design of a low-noise amplifier for an IEEE802.11a wireless communication receiver

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Design of a low-noise amplifier for an IEEE802.11a wireless communication receiver

by

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A dissertation submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Major: Electrical Engineering (Microelectronics)

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Iowa State University

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2004

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Signature was redacted for privacy.

Major Professor

Signature was redacted for privacy.

For the Major Program

To my family

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ACKNOWLEDGMENTS

I would like to thank many people who made my life at Iowa State University so memorable and continuously encouraged me to complete my study toward my Ph.D.

First and foremost, I would like to express my sincere gratitude to my major professor, Prof. Robert J. Weber, for his guidance and support during my PhD study. He has been a great research mentor with a lot of enthusiasm, establishing an exceptional example of a senior scientist and engineer. His continuous encouragement and attitude have been of great help to me to resolutely pursue the true answers to unsolved problems in my research.

I am indebted to Dr. Julie Dickerson for her continuous support of this work. It is under her guidance that I began to understand the communication basics and the associated signal process techniques. The valuable knowledge I learnt from her has facilitated my research on the wireless communication system design.

I also would like to thank my committee members for their time and help. I would like to thank Dr. Jiming Song, who has spent a lot of time on my dissertation and did not neglect any slight ambiguity in expression. I would like to thank Dr. Huaiqing Wu, whose suggestions helped me establish the correct equations for the multi-port noise analysis. Without discussions with him, the multi-port noise analysis would not have been possible. I also would like to thank Dr. Gary Tuttle, who helped me test and debug the chips. I would like to thank Dr. Chris Chong-Nuen Chu for his guidance on interconnection issues and estimation of interconnection inductance.

Finally, I would like to give many thanks to my beloved wife, Haiyan Sun, for her love that has always encouraged me. I must reserve special thanks to my mom, Yuehua Cai. Without her support, I would not have been able to come this far.

ABSTRACT

Wireless communication and its applications have been growing rapidly in recent years. The driving force behind this development is the introduction of Digital Signal Processing (DSP) in the wireless communication world. While DSP functionality is highly integrated using Complementary Metal-Oxide-Semiconductor (CMOS) technology, current Front-End (FE) Integrated Circuits (ICs) depend on a mixture of semiconductor technologies, from GaAs to SiGe, making integration of the whole communication system on a single chip almost impossible. With the recent advance in CMOS technology, Radio Frequency (RF) CMOS IC design provides a potential solution for System-On-Chip (SOC).

This dissertation explores the design of a fully integrated CMOS Low-Noise Amplifier (LNA) for an IEEE 802.11a wireless communication receiver. A new design methodology is presented for optimization of feedback to achieve simultaneous noise and gain match. Two-port noise theory is extended to multi-port noise analysis for a three-port-to-two-port noise transformation. This approach is applied in the design of a 5.3-GHz LNA in a CMOS 0.18-um technology. The measurement gives averagely forward gain of 5.2 dB, input and output impedance matching of –9.3 dB and –8.9 dB respectively, isolation of –42.8 dB, estimated noise figure of 4.8 dB at frequency of 5.3-GHz with current consumption of 4.2-mA from a 1.5-V supply. A novel process-variation insensitive network is proposed to realize the on-chip impedance matching that is immune to process variation. The proposed network utilizes precision matching capacitors to achieve a zero sensitivity to process variation. Its performance is demonstrated in Monte Carlo simulations.

CHAPTER 1. INTRODUCTION

1.1 Problem Statement

Immersive virtual environments have been moving from primarily research test-beds to practical systems used as research and development tools in many science domains. However, current technologies impose limitations on how the users move and interact in these environments. For example, in the C2 system at Iowa State University (ISU), which is a 3-sided and a floor projection environment, many devices are tethered. The tethered cables put a significant physical constraint on where and how users can move in this semi-closed projection cube.

In the current C6 system, which is an enclosed 6-sided immersion environment, the cables are replaced with wireless links with the help of recent advancements in the wireless communication world. The wireless solution, however, brings in other design considerations. Wireless systems are susceptible to noise and interference as compared to the wired system. This leads to issues of reliability and latency in the virtual reality (VR) environment. For the immersive VR system to respond promptly to the user's interaction, the data transmission through the wireless links should satisfy a number of specifications regarding speed, latency, reliability, etc. There are now many commercial wireless devices used in the C6 system, with operation bands ranging from DC magnetic field to 2.4 GHz. Not all of these off-shelf products are customized to meet the data transmission requirements in the C6 system.

As more devices are involved in the C6 system, more wireless links will be introduced, leading to a more crowded medium for wireless communication. Each individual wireless

link is an interference to the rest. One link can be strong enough to disable some of the other wireless links. In addition, each wireless product consumes a certain amount of power. More devices mean more power consumption that directly leads to either a heavier user-carried battery or a shorter lifetime of operation. Therefore, there exists a need to customize the wireless design in the current C6 system.

This dissertation will study the feasibility of a single highly integrated low-power high-speed wireless solution that can be used as a replacement for the current wireless systems and can be extended for future use as well.

1.2 Scope of the Dissertation

Wireless communications and their application have been growing rapidly in recent years. The driving force behind this development is the introduction of digital signal processing (DSP) in the wireless communication world. While DSP functionality is highly integrated using CMOS technology, current front-end analog circuits depend on a mixture of semiconductor technologies, from GaAs to SiGe, making integration of the whole communication system on a single chip almost impossible. With recent advancements in CMOS technology, Radio Frequency (RF) CMOS Integrated Circuit (IC) design provides a potential solution for System-On-Chip (SOC).

This dissertation will present a low-noise amplifier (LNA) for a wireless communication receiver compatible with IEEE 802.11a protocol as part of a wireless solution for the current C6 immersive system. Receiver link budget analysis and system design will be presented in Chapter 2. Multi-port noise analysis extended from the two-port noise theory will be discussed in Chapter 3. Chapter 4 will focus on a new design methodology of the low-noise

amplifier employing the presented multi-port noise analysis. Measurement and testing results will be listed and discussed in this chapter as well. A novel impedance matching network that is insensitive to process variation will be analyzed in Chapter 5. Chapter 6 will summarize and conclude the current work and identify future work.

CHAPTER 2. SYSTEM DESIGN FOR IEEE 802.11A APPLICATIONS

2.1 Introduction

For replacement of current wireless links in the C6 system, the proposed wireless solution should have the following features: high speed, low power, low latency and compatibility.

There are currently two competing wireless specifications, Bluetooth and IEEE 802.11, for short-range wireless applications. Bluetooth was initiated to replace the cables from the computers to printers, network jacks, etc. Currently, it has evolved into a personal wireless network protocol with a coverage area in the general vicinity of the user. IEEE 802.11 was initially a specification for Wireless Local Access Networks (WLANs) [2.1].

The Bluetooth specifications are aimed to be a low-cost, power-efficient, single radio-chip solution in the 2.4-GHz industrial, scientific and medical (ISM) band. The original proposed modulation rate is 1M symbol per second. The symbol rate is equal to the bit rate because the modulation scheme is Gaussian Frequency Shifting Keying (GFSK). So the maximum available bit rate is 1 Mbps. In addition, the network structure utilizes a star-shaped configuration in which the device at the center performs the role of master and all other devices, up to seven, operate as slaves. This structure is called piconet. The star-shaped configuration puts further limits on the data rate [2.2]. Furthermore, the 2.4-GHz band suffers from many other interference sources, such as microwave ovens. Therefore, the Bluetooth protocol is not a suitable candidate for the C6 system.

IEEE 802.11a, an extension of the IEEE 802.11 specifications in the 5-GHz unlicensed national information infrastructure (U-NII) bands, provides a variety of data rates ranging from 6 Mbps to 54 Mbps [2.3]. Acceptable latency thresholds can be achieved [2.1]. Power consumption can be optimized with customized design for this global standard.

By comparing current wireless communication specifications, it can be seen that the IEEE 802.11a protocol provides a feasible wireless solution to the C6 system. Slight modifications are necessary to make it meet the special needs of low power and low latency imposed by the VR system.

The following sections will discuss the analysis and design of a receiver system for the IEEE 802.11a specification.

2.2 Receiver Link Budget Analysis

To derive requirements for the receiver system and its building blocks, the following specifications from the IEEE 802.11a protocol are used with customized modifications.

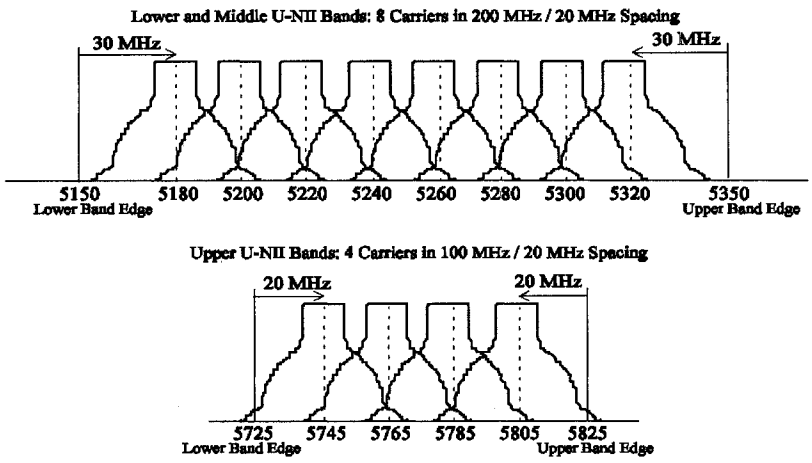

Figure 2-1. U-NII band frequency channel plan for the United States [2.3].

As can be seen in Figure 2-1, the U-NII band has three sub bands. The lower band is from 5.15-GHz to 5.25-GHz; the middle band is from 5.25-GHz to 5.35-GHz, and the upper band is from 5.725-GHz to 5.825-GHz. The lower and middle bands are used since eight channels are provided. The channel bandwidth (BW) is 20 MHz.

Table 2-1 below summarizes the specifications used to conduct the link budget analysis.

Table 2-1. Receiver specifications compatible to IEEE 802.11a for the C6 system [2.3]

	Specifications	Value	Description
IEEE spec.	f	5.15 to 5.35 GHz	Frequency range
	BW	20 MHz	Bandwidth
	DataR	18 Mbps	Data rate
	Modulation	QPSK	Modulation scheme
	$P_{RX(min)}$	-77 dBm	Minimum sensitivity
	$P_{TX(max)}$	23 dBm	Maximum transmitted power
	P_{ADJ}	-50 dBm	Adjacent channel power
C6 spec.	BER	10^{-5}	Bit error rate
	E_B/N_o	10.5 dB	Bit energy to noise ratio
	R	20 m	Transmission range
	FadeM	20 dB	Fading margin
	G_T	2.41 dB	TX antenna gain (dipole)
	G_R	2.41 dB	RX antenna gain (dipole)

The specifications for the C6 system are to provide a data rate of 18 Mbps. To achieve a BER of 10^{-5} with a QPSK modulation scheme, the E_B/N_o is found to be at least 12.6 dB [2.4]. The transmission range, which is the distance between the transmitter and the receiver, is assumed to be 20 m that will provide sufficient coverage for the C6 system of which the cube is a 10 by 10 by 10-foot arena.

The following calculations for the link budget analysis are based on [2.5].

The first step is to find the free space loss, L_{FS}, with a range of 20 m as

$$L_{FS} = 20*\log_{10}\left(\frac{4\pi*R}{\lambda}\right) = 20*\log10\left(\frac{4\pi*R*f_{\max}}{c}\right)$$
$$= 20*\log_{10}\left(\frac{4\pi*20*5.35e9}{3e8}\right) = \underline{\underline{73.0\,dB}} \qquad (2\text{-}1)$$

As can been in Figure 2-2, at 2.4 GHz the indoor space loss is about 3 dB higher than the free space loss at a distance of 20 m (65.6 ft). It is assumed at 5 GHz that the indoor space loss will be about 3 to 6 dB higher at the same distance. 6 dB is used for a better design margin. So the total loss, L_t, is found to be 79.0 dB.

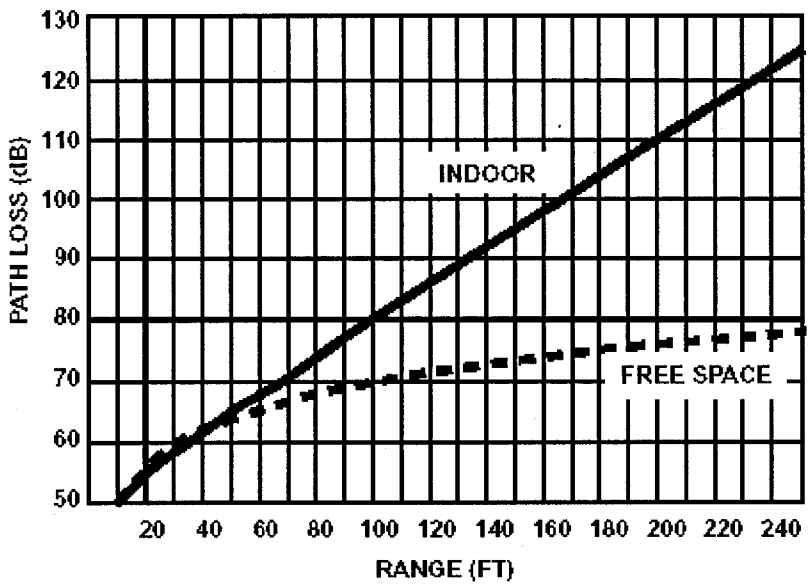

Figure 2-2. Estimated indoor propagation losses at 2.4 GHz [2.5].

Using this total loss the minimum transmitted power is found to be

$$P_{TX\,(\min)} = P_{RX\,(\min)} - G_T - G_R + L_t + FadeM$$
$$= -77\,dBm - 2.41\,dBi - 2.41\,dBi + 79\,dB + 20\,dB = \underline{\underline{17.2 \quad dBm}} \qquad (2\text{-}2)$$

This minimum transmitted power is less than the maximum power (23 dBm) permitted by the FCC regulation in this band.

To calculate the maximum received power at the input of the receiver, the free space loss at a minimum distance of 2-m between the transmitter and the receiver is

$$L_{FS(\min)} = 20*\log 10\left(\frac{4\pi*2*5.15e9}{3e8}\right) = \underline{\underline{53.0 \quad dB}} \tag{2-5}$$

Using the minimum loss and the maximum transmitter power (FCC regulations) the maximum input power of the receiver is

$$\begin{aligned} P_{RX(\max)} &= P_{TX(\max)} + G_T + G_R - L_{FS(\min)} - FadeM \\ &= 23dBm + 2.41dBi + 2.41dBi - 53dB - 20dB \cong \underline{\underline{-45.0 \quad dBm}} \end{aligned} \tag{2-6}$$

So the receiver must be able to cope with a signal with power level up to –45 dBm.

The signal-to-noise ratio (SNR) is calculated to be

$$\begin{aligned} SNR &= \frac{E_B}{N_O} + 10*\log 10\left(\frac{DataR}{BW}\right) \\ &= 10.4dB + 10*\log 10\left(\frac{18e6}{20e6}\right) = \underline{\underline{10.0 \quad dB}} \end{aligned} \tag{2-7}$$

Using this SNR, the input referred noise figure (NF) for the receiver is found to be

$$\begin{aligned} NF_{RX} &= P_{RX(\min)} - SNR + KT - 10*\log 10(BW) \\ &= -77dB - 10.0dB + 174dBm/Hz - 10*\log 10(20e6) = \underline{\underline{14.0 \quad dB}} \end{aligned} \tag{2-8}$$

To avoid inter-modulation problems with adjacent cannels, the minimum input referred third order intercept point (IIP3) is found

$$\begin{aligned} IIP3 &= P_{ADJ} + \frac{P_{ADJ} - P_{RX(\min)} + SNR}{2} \\ &= -50dBm + \frac{-50dBm - (-77dBm) + 10.4dB}{2} = \underline{\underline{-31.0 \quad dBm}} \end{aligned} \tag{2-9}$$

2.3 Receiver Architecture Design

The receiver architecture is chosen to be a super-heterodyne structure, as illustrated in Figure 2-3. This traditional structure will provide more design flexibility than a direct conversion structure, although some off-chip IF filters are necessary.

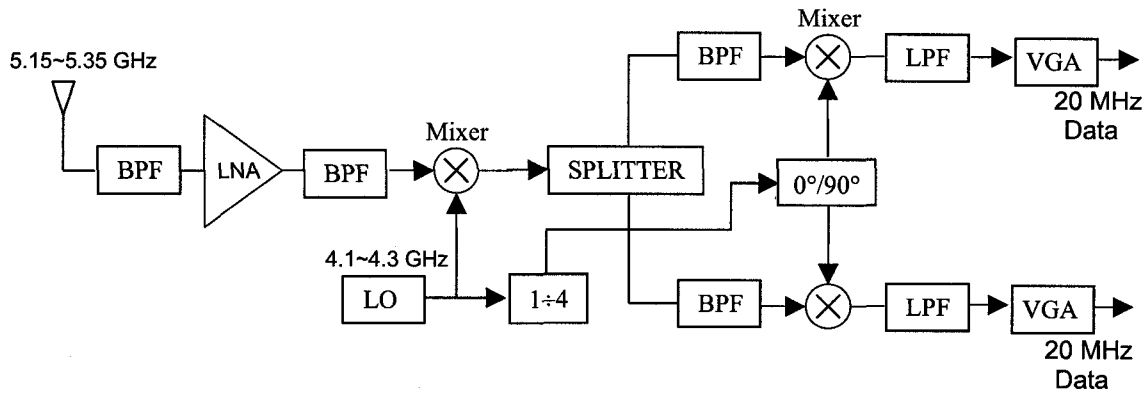

Figure 2-3. A super-heterodyne receiver structure for IEEE 802.11a applications.

The proposed frequency plan for the dual down-conversion is shown in Figure 2-4. The second local oscillator frequency is chosen to be a quarter of the first local oscillator frequency, i.e., $LO_2 = LO_1/4$. Thus only one frequency synthesizer is needed.

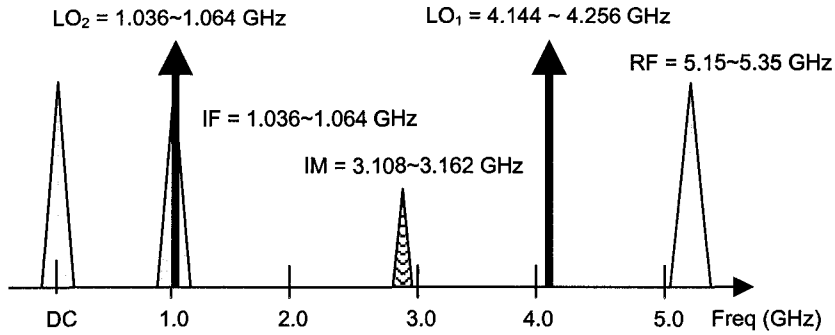

Figure 2-4. Proposed frequency plan for dual down-conversion.

Table 2-2. Frequency plan for dual down-conversion

	Frequency	Channel spacing
RF signal	5.150 ~ 5.350 GHz	20 MHz
LO_1 signal	4.144 ~ 4.256 GHz	16 MHz
LO_2 signal	1.036 ~ 1.064 GHz	4 MHz

The noise figure and IIP3 given above are distributed among the front-end components of filters, amplifiers and mixers, etc. The following equations were used to find the input referred contributions of NF and IIP3. The specifications for each building block are listed in Table 2-3.

$$NF_{IN} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \frac{NF_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{NF_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{2-10}$$

$$\frac{1}{IIP3_{IN}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \frac{G_1 G_2 G_3}{IIP3_4} + \cdots + \frac{G_1 G_2 \cdots G_{n-1}}{IIP3_n} \tag{2-11}$$

Table 2-3. Circuit specifications

	BPF (1)	LNA	BPF (2)	Mixer (1)	Splitter	BPF (3)	Mixer (2)	LPF	VGA	Total	Spec.
Gain (dB)	-3.0	15.0	-3.0	6.0	-3.0	-3.0	8.0	-2.0	62.0	77	
NF (dB)	3.0	3.0	3.0	8.0	3.0	3.0	10.0	2.0	10.0	7.7	*14.0*
IIP3 (dBm)		-20.0		-15.0			-10.0			-24.8	*-31.0*

Using the gain values in Table 2-3, the dynamic range needed from the variable-gain amplifier (VGA) can be found. In doing this calculation it is assumed that the ADC input requires a 0-dB signal.

$$\begin{aligned} G_{VGA(\max)} &= P_{ADC} - P_{RX(\min)} - RF\_Gain \\ &= 0dB - (-77dBm) - 15dB = \underline{\underline{62.0\ \ dB}} \end{aligned} \tag{2-12}$$

$$\begin{aligned} G_{VGA(\min)} &= P_{ADC} - P_{RX(\max)} - RF\_Gain \\ &= 0dB - (-45dBm) - 15dB = \underline{\underline{30.0\ \ dB}} \end{aligned} \tag{2-13}$$

$$DR_{VGA} = G_{VGA(\max)} - G_{VGA(\min)} = 62dB - 30dB = \underline{\underline{32.0 \quad dB}} \tag{2-14}$$

2.4 System Simulations

The proposed receiver structure and specifications were implemented in SystemView™, a communication system simulator. The block diagram of the simulator in SystemView™ is shown in Figure 2-5. The simulator consists of three parts: Transmitter (TX), Channel (Chn), Receiver (RX).

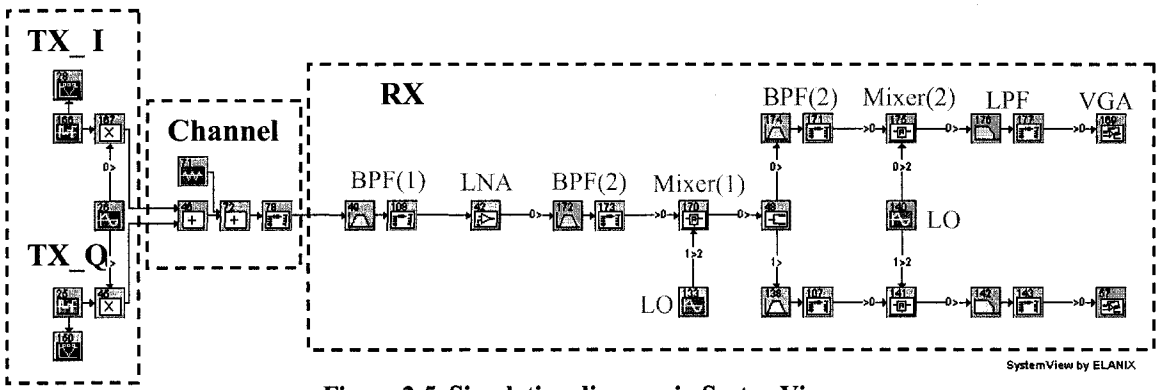

Figure 2-5. Simulation diagram in SystemView.

The TX is an ideal transmitter to generate in-phase and quadrature bit streams for testing purposes. Two pseudo-noise (PN) coders generate two 18-Mbps digital signals that are modulated by the quadrature modulator to the desired frequencies. These two signals are then summed for transmission through the channel.

The channel is modeled using a thermal noise generator and an attenuator. The thermal noise generator adds white additive Gaussian noise (WAGN) to the transmitted signal to simulate a desired SNR. The noise level is determined by its internal setting of noise temperature. The attenuator is used to model the path loss of the channel.

The RX has in-phase and quadrature signal paths. First, the signal passes through the BPF(1) that limits the bandwidth to 5.0~5.5 GHz. Each filter is followed by an attenuator to model the filter loss. The antenna model is absorbed into the attenuator in the channel model. After the BPF(1), the signal is amplified by the LNA to a certain power level. Then it passes through the BPF(2) for harmonic removal before being processed by the active mixer(1). An splitter is necessary to separate the RF signal into two signal paths for individual signal processing. The active mixer(2) down-converts the RF signal to a base-band signal. A LPF then rejects the adjacent channels by 35 dB to minimize interference. The last component in the simulator is a VGA used to amplify the signal to the desired level to meet the dynamic requirement of the ADC.

Channel 4 with a center frequency of 5.240 GHz is chosen for simulation purposes. Accordingly, LO_1= 4.192 GHz, LO_2 = 1.048 GHz. The simulation results are shown below in Figure 2-6 and Figure 2-7.

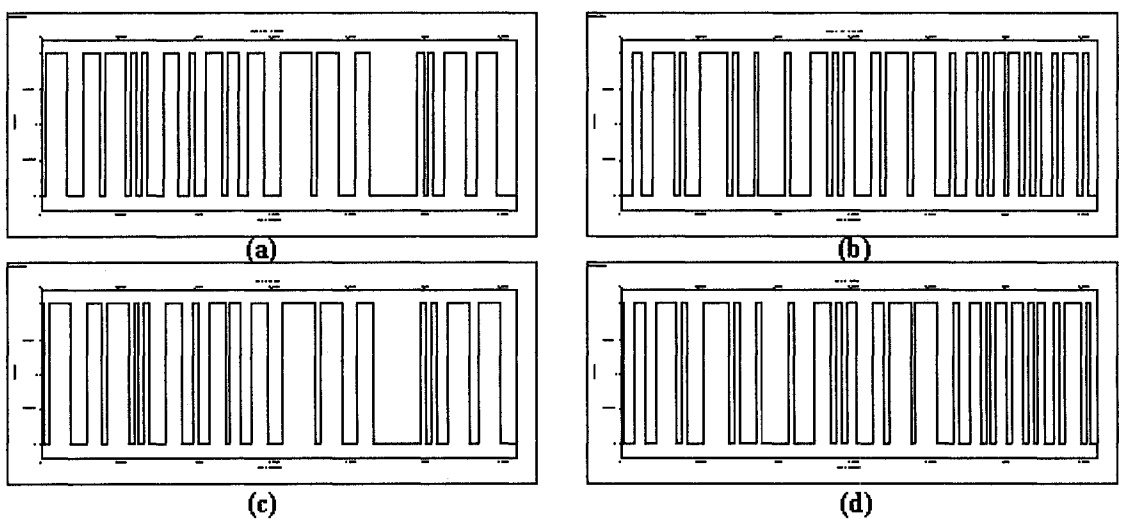

Figure 2-6. Simulation results (a) Tx_I data, (b) Tx_Q data, (c) Rx_I data, (d) Rx_Q data.

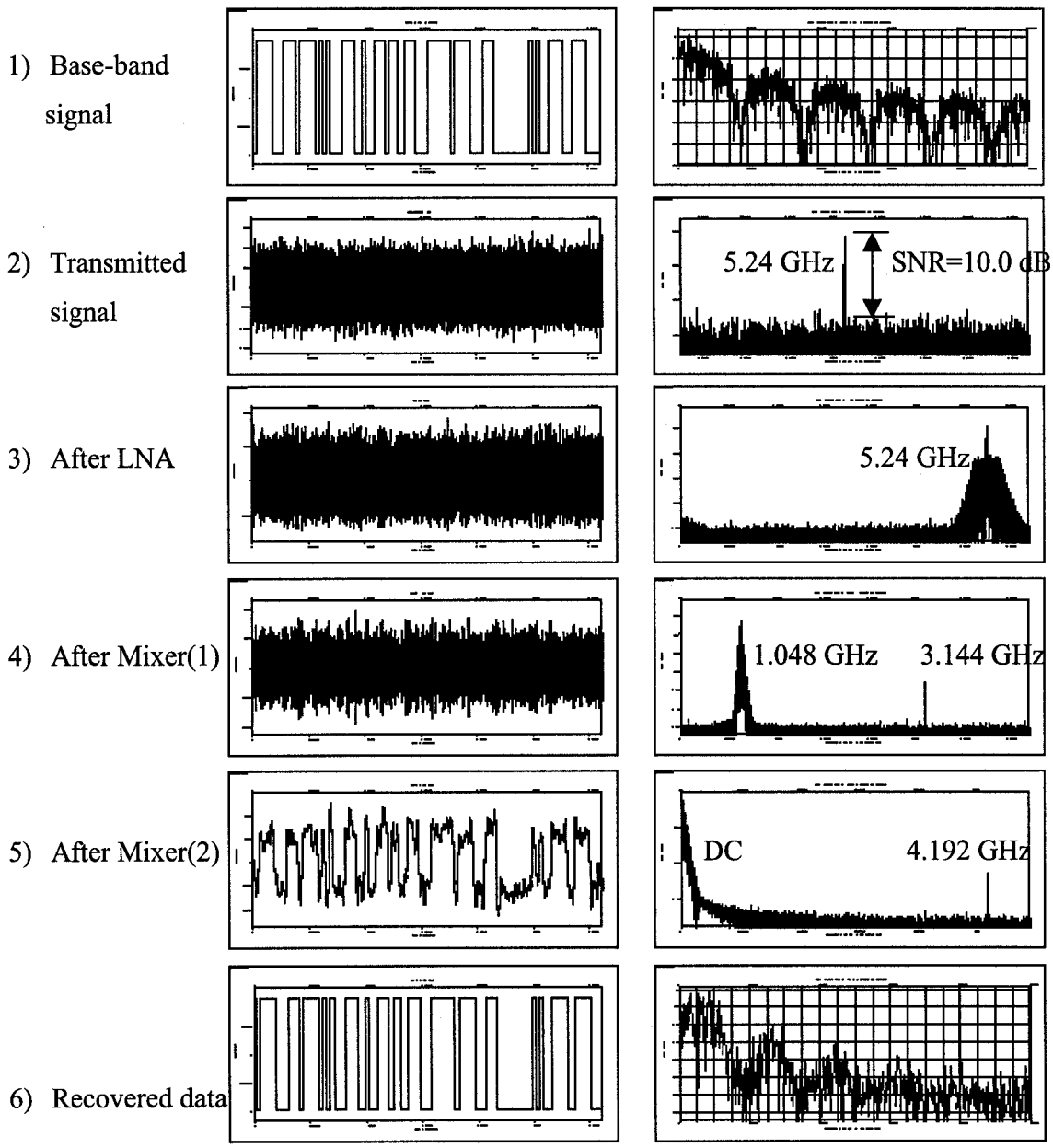

Figure 2-7. Simulation results (a) time domain, (b) spectrum.

From the simulation results it can be seen that the implemented receiver can recover the transmitted data without error. Combinations of different input power levels and channel attenuations are verified by the simulator as well.

2.5 Conclusions

A set of receiver specifications compatible with IEEE 802.11a protocols is proposed with the design customized for the immersive C6 system. Based on the link budget analysis, the receiver system requirements, such as NF, IIP3, are derived. A super-heterodyne architecture is proposed with a corresponding frequency plan. Specifications for the building blocks in the receiver system are derived. The receiver architecture and the circuit specifications are verified using SystemView.

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CHAPTER 3 . MULTI-PORT NOISE ANALYSIS

3.1 Introduction

Noise transformation of a linear noisy two-port circuit with either feedback or another linear noisy two-port has been established in [3.1, 3.2, 3.3] based on the well-known two-port noise theory in [3.4].

A MOSFET is a three-terminal device, not considering the body contact that is usually tied to the substrate. When one of its three terminals (gate, drain and source) is DC or AC grounded as a common terminal, the MOSFET can be treated as a two-port circuit. Thus the two-port noise transformation can be used when series or shunt feedback is applied to the other two terminals.

In the design of an LNA, a source-degeneration inductor, L_s, is usually presented in the first stage of a common-source MOSFET for both noise and input impedance match [3.5, 3.6]. In this case, the utilized two-port S matrix and the two-port noise parameters are not sufficient to model the behavior of the MOSFET with the source terminal not grounded, because they are extracted with the condition of a grounded source terminal. Therefore, the two-port noise transformations are not valid in evaluating the effect of L_s on two-port noise parameters. Instead, a three-port approach should be employed.

In this chapter the two-port noise theory will be extended to a three-port noise analysis that utilizes a three-port noise matrix in [3.7] to characterize the noise behavior of a MOSFET. An explicit formulation is given for its noise transformation when one of the three ports is terminated with a certain impedance as feedback to form a two-port circuit and the

result is verified with circuit simulations. De-embedding a three-port noise matrix from two-port circuit simulations is also demonstrated. Then the three-port noise analysis is generalized to a multi-port noise analysis for the investigation of multiple feedback on multi-port networks.

3.2 Two-Port Noise Theory for Linear Noisy Two-Port Networks

The two-port noise theory in [3.4], the basis of the multiple noise analysis, is briefly introduced in this section to facilitate the understanding of the following sections.

The electrical behavior of a linear noisy two-port network as shown in Figure 3-1 can be described by two linear equations between the input and output voltages and currents. Here and thereafter the Y-admittance matrix is chosen to represent the linear network. The relations between voltages and currents are given as

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-1}$$

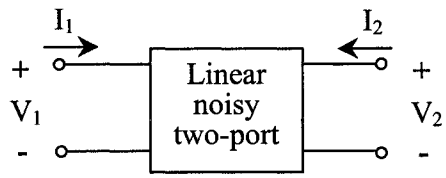

Figure 3-1. A linear noisy two-port network.

The internal noise sources of the two-port network are represented by two external equivalent noise current sources, i_1 and i_2. The equivalent circuit with external noise current sources is shown in Figure 3-2. It is worth pointing out that i_1 and i_2 are correlated to each other because they may refer to the same internal noise sources.

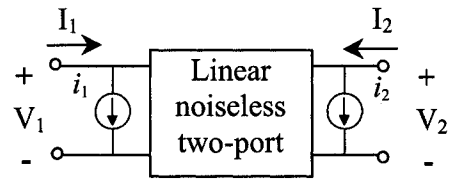

Figure 3-2. An equivalent circuit with external noise current sources of i_1 and i_2.

It is more convenient to use input-referred noise sources in noise analysis. Re-arranging (3-1) gives

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} -\frac{Y_{22}}{Y_{21}} & \frac{1}{Y_{21}} \\ Y_{12} - \frac{Y_{11}Y_{22}}{Y_{21}} & \frac{Y_{11}}{Y_{21}} \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} + \begin{pmatrix} -\frac{1}{Y_{21}} i_2 \\ i_1 - \frac{Y_{11}}{Y_{21}} i_2 \end{pmatrix} \tag{3-2}$$

Define $u = -\frac{1}{Y_{21}} i_2$ and $i = i_1 - \frac{Y_{11}}{Y_{21}} i_2$. (3-2) can be written as

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} -\frac{Y_{22}}{Y_{21}} & \frac{1}{Y_{21}} \\ Y_{12} - \frac{Y_{11}Y_{22}}{Y_{21}} & \frac{Y_{11}}{Y_{21}} \end{pmatrix} \begin{pmatrix} V_2 \\ I_2 \end{pmatrix} + \begin{pmatrix} u \\ i \end{pmatrix} \tag{3-3}$$

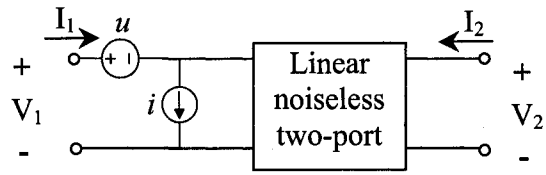

Figure 3-3. An equivalent circuit with input-referred noise sources of *u* and *i*.

The input-referred noise sources are modeled as the noise voltage source u and the noise current source i, as shown in Figure 3-3. Normally u and i are correlated to each other. The noise current source i can be divided into two parts with one part, i_n, not correlated to u, while the other part is fully correlated to u. The correlation coefficient is represented by the correlation admittance Y_{cor}. The relationship can be written as

$$i = i_n + Y_{cor} \cdot u \tag{3-4}$$

where

$$Y_{cor} = G_{cor} + j \cdot B_{cor} \tag{3-5}$$

The equivalent circuit in Figure 3-3 can be further decomposed into Figure 3-4 using (u, i_n, Y_{cor}). The four components, u, i_n, and the real and imaginary parts of Y_{cor}, can fully describe the noise behavior of a linear noisy two-port network and are named as four noisy poles.

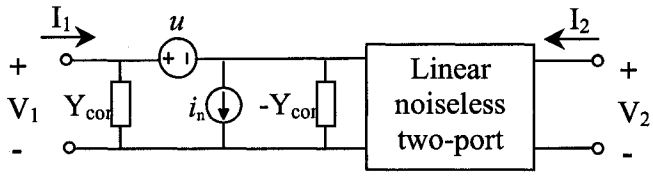

Figure 3-4. An equivalent circuit with input-referred noise sources of u and i_n.

The correlation admittance Y_{cor} is noiseless. The noise sources u and i_n are characterized by the Nyquist formulas using the equivalent noise resistance R_n and the equivalent noise conductance G_n respectively as

$$\overline{|u|^2} = \overline{u \cdot u^*} = 4kT\Delta f \cdot R_n \tag{3-6}$$

$$\overline{|i_n|^2} = \overline{i_n \cdot i_n^*} = 4kT\Delta f \cdot G_n \tag{3-7}$$

where k is Boltzman constant, T is absolute temperature, Δf is the bandwidth. R_n, G_n together with Y_{cor} can fully characterize the noise behavior of a linear noisy two-port network.

In reality, the noise characteristics of a two-port network are measured based on another set of four noise parameters: the minimum noise factor F_{min}, the equivalent noise resistance R_n, and the optimum source admittance Y_{opt} with $Y_{opt} = G_{opt} + j \cdot B_{opt}$.

Therefore, there are several representations for the noise behavior of a two-port network: $\{\overline{|i_1|^2}, \overline{|i_2|^2}, \overline{i_1 i_2^*}\}$, $\{\overline{|u|^2}, \overline{|i_n|^2}, Y_{cor}\}$, $\{R_n, G_n, Y_{cor}\}$ or $\{F_{min}, R_n, Y_{opt}\}$. These representations are equivalent to each other. Conversion equations in [3.4] are summarized as

$$\begin{pmatrix} u \\ i \end{pmatrix} = \begin{pmatrix} 0 & -1/Y_{21} \\ 1 & -Y_{11}/Y_{21} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-8}$$

$$\begin{pmatrix} u \\ i_n \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ -Y_{cor} & 1 \end{pmatrix} \begin{pmatrix} u \\ i \end{pmatrix} = \begin{pmatrix} 0 & -1/Y_{21} \\ 1 & Y_{cor} - Y_{11}/Y_{21} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-9}$$

$$\begin{aligned} F_{\min} &= 1 + 2(\sqrt{G_{cor}^2 + G_n / R_n} + G_{cor}) R_n \\ Y_{opt} &= \sqrt{G_{cor}^2 + G_n / R_n} - jB_{cor} \end{aligned} \tag{3-10}$$

$$\begin{aligned} Y_{cor} &= (F_{\min} - 1)/(2R_n) - G_{opt} - jB_{opt} \\ G_n &= (G_{opt}^2 - [(F_{\min} - 1)/(2R_n) - G_{opt}]^2) R_n \end{aligned} \tag{3-11}$$

$$\begin{aligned} \overline{|i_1|^2} &= |Y_{cor} - Y_{11}|^2 \cdot \overline{|u|^2} + \overline{|i_n|^2} \\ \overline{|i_2|^2} &= |Y_{21}|^2 \cdot \overline{|u|^2} \\ \overline{i_1 i_2^*} &= (Y_{11} - Y_{cor}) \cdot Y_{21}^* \cdot \overline{|u|^2} \end{aligned} \tag{3-12}$$

$$\overline{|u|^2} = \overline{|i_2|^2} \Big/ |Y_{21}|^2$$

$$\overline{|i_n|^2} = \overline{|i_1|^2} - \overline{i_1 i_2^*}^2 \Big/ \overline{|i_2|^2} \tag{3-13}$$

$$Y_{cor} = Y_{11} - Y_{21} \cdot i_1 i_2^* \Big/ |i_2|^2$$

Noise factor (F), or Noise Figure (NF), is a measure that quantitates the noise performance of a circuit by representing the degradation of the signal-to-noise ratio due to the circuit.

$$F \equiv \frac{\left(S/N\right)_{in}}{\left(S/N\right)_{out}} = \frac{Total\ \ available\ \ output\ \ noise}{Output\ \ noise\ \ available\ \ from\ \ the\ \ source} \tag{3-14}$$

$$NF = 10\log_{10}(F) \tag{3-15}$$

The noise factor of a two-port circuit in Figure 3-5 is given by

$$F = F_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{opt}\right|^2 = F_{min} + \frac{R_n}{G_s}\left[\left(G_s - G_{opt}\right)^2 + \left(B_s - B_{opt}\right)^2\right] \tag{3-16}$$

where $Y_S = G_S + jB_S$ is the source admittance.

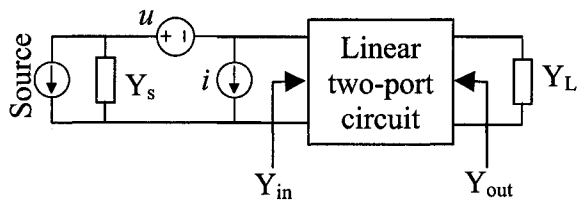

Figure 3-5. An input-referred noise model for a linear noisy two-port circuit.

When Y_s is equal to Y_{opt}, the noise factor reaches its minimum, F_{min}. This condition is called noise match. Any mismatch between Y_s and Y_{opt} will yield a larger noise factor.

When the input admittance Y_{in}, which is a function of the load admittance of Y_L, is equal to the conjugate of the source admittance Y_s, the input port is impedance matched. If the output admittance Y_{out}, which is a function of the source admittance Y_s, is equal to the conjugate of the load admittance Y_L, the output port is impedance matched. If the linear two-port circuit is unconditionally stable, a unique pair of Y_s and Y_L exists that simultaneously satisfies input and output impedance match, which is called Simultaneous Conjugate Match (SCM). In this condition, the transducer gain G_T is optimized to maximum stable transducer gain G_{Tmax} [3.8]. The source and load admittances for SCM are noted as $Y_{s,SCM}$, $Y_{L,SCM}$.

In many CMOS RF circuits without feedback, $Y_{s,SCM}$ is significantly different from Y_{opt}, which means minimum noise figure and maximum transducer gain can not be achieved simultaneously. If the source admittance is matched for minimum noise figure, transducer gain is much lower than G_{Tmax}, and vice versa. Design trade-offs may exist for acceptable noise figure and transducer gain. However, simultaneous noise match and impedance match at input and output ports are ideal.

To achieve simultaneous noise and power match, noiseless feedback can be applied to modify the network to bring Y_{opt} close to $Y_{s,SCM}$, as shown in Figure 3-6. Noise transformation of a linear noisy two-port circuit with either feedback or another linear noisy two-port has been established in [3.1, 3.2, 3.3].

The previous developed noise transformation is based on the two-port noise theory. The original network should remain as a two-port circuit when either shunt or series feedback is applied. If this condition is violated, the two-port noise transformation will not hold.

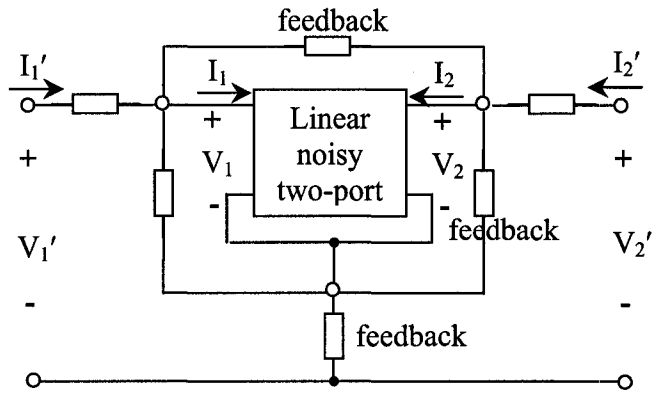

Figure 3-6. A linear two-port network with series and shunt feedback

In the design of a CMOS LNA, a source-degeneration inductor, L_s, is usually present in the first stage of a common-source MOSFET for both noise and input impedance match [3.5, 3.6]. In this case, this MOSFET should be treated as a three-port circuit because its source terminal is not AC grounded when L_s is presented. Two-port noise transformations are not valid in evaluating the effect of L_s on the four two-port noise parameters, because the two-port Y matrix and the two-port noise parameters extracted under the condition of a grounded source terminal are not sufficient to model the behavior of the MOSFET with the source terminal not grounded. Instead, a three-port approach should be employed.

The reason can be further explained with the view of an equivalent three-port model as shown in Figure 3-7. A three-port circuit can be modeled by a three-port Y matrix and three external equivalent noise currents, i_1, i_2 and i_3. When it is treated as a two-port circuit with the third port shorted to ground, the resultant two-port network can be represented by a two-port Y matrix and two-port noise parameters, but these two-port data do not include the equivalent parameters associated with the third port. When feedback is applied to the third port, these equivalent parameters at the third port are brought into the circuit. Therefore, the

two-port Y matrix and two-port noise parameters are not valid to represent the three-port circuit with one port terminated with feedback.

Therefore, a three-port noise analysis is necessary to analyze the feedback effect on the two-port noise parameters for a three-port network. Noise transformations based on three-port noise analysis will be presented in the following sections and then generalized to a multi-port noise analysis.

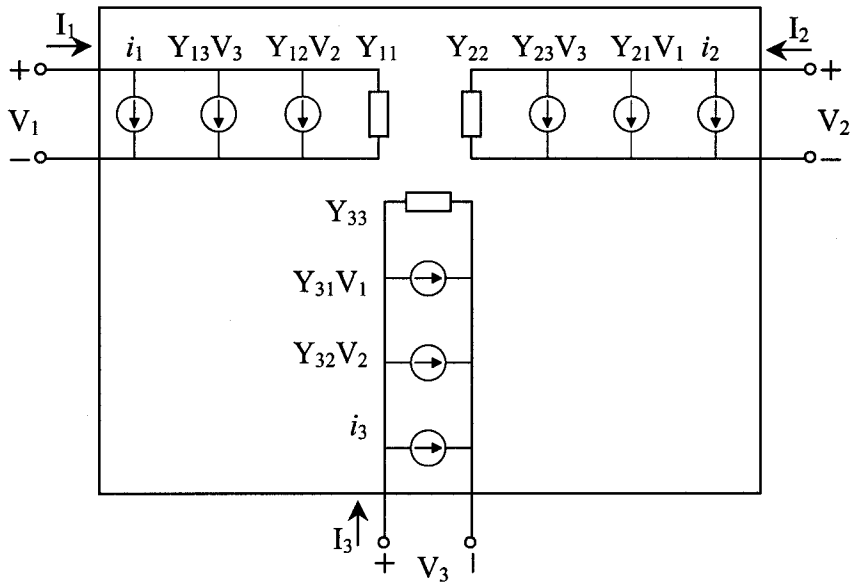

Figure 3-7. An equivalent circuit of a linear noisy three-port network.

3.3 Three-Port Noise Analysis

3.3.1 *Noise Matrix*

A linear noisy three-port network can be characterized by either its admittance matrix Y and three equivalent noise current sources, i_1, i_2 and i_3, or its impedance matrix Z and three equivalent noise voltage sources u_1, u_2 and u_3 [3.7]. These two representations are equivalent

to each other. In this paper the former one is used, as shown in Figure 3-8, for reasons of ease of de-embedding the three-port noise matrix from two-port circuit simulations.

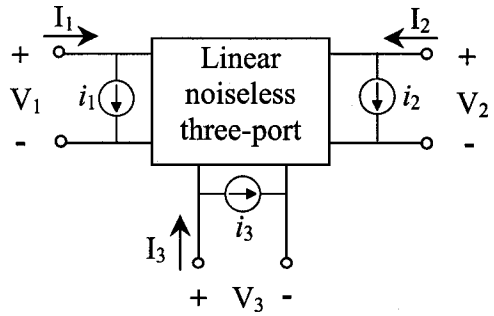

Figure 3-8. An equivalent representation of a linear noisy three-port network with internal noise sources.

The analytical relation between voltages and currents applied to the three ports can be written as

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} \tag{3-17}$$

The corresponding noise current matrix can be written as [3.7]

$$\mathbf{N} = \overline{\mathbf{i}\mathbf{i}^{\mathrm{H}}} = \begin{pmatrix} \overline{i_1 i_1^*} & \overline{i_1 i_2^*} & \overline{i_1 i_3^*} \\ \overline{i_2 i_1^*} & \overline{i_2 i_2^*} & \overline{i_2 i_3^*} \\ \overline{i_3 i_1^*} & \overline{i_3 i_2^*} & \overline{i_3 i_3^*} \end{pmatrix} \tag{3-18}$$

The noise current matrix has nine entities $\overline{|i_1|^2}$, $\overline{|i_2|^2}$, $\overline{|i_3|^2}$ and the real and imaginary parts of $\overline{i_1 i_2^*}$, $\overline{i_1 i_3^*}$, $\overline{i_2 i_3^*}$. For a linear noisy two-port, the rank of both admittance and noise matrices is reduced to two. The noise current matrix will have four entities: $\overline{|i_1|^2}$, $\overline{|i_2|^2}$ and the real and imaginary parts of $\overline{i_1 i_2^*}$.

3.3.2 *Extraction of Three-port Noise Matrix*

Current EDA tools support only two-port noise analysis in circuit simulations. A set of four noise parameters is given as minimum noise factor F_{min}, equivalent noise resistance R_n, and optimum source impedance reflection coefficient Γ_{opt}. This set of four noise parameters is equivalent to other noise parameter representations such as the noise current matrix or the four noise parameters $\{R_n, G_n, Y_{cor}\}$ in [3.4]. Conversion among these representations can be done using equations in [3.4].

A three-port network can be reduced to a two-port by shorting one of the three ports. By doing this, the noise current at the shorted port is not involved in the two-port noise analysis. This is shown in a later section. Thus, a corresponding circuit simulation of the resultant two-port will give $\{F_{min}, R_n, \Gamma_{opt}\}$ that can be converted to $\{\overline{|i_k|^2}, \overline{|i_\ell|^2}, \overline{i_k i_\ell^*}\}$, where $k, \ell = 1,2,3$ and $k \neq \ell$. Therefore a three-port noise matrix can be extracted from three sets of two-port circuit simulations by shorting each of the three ports respectively.

3.3.3 *Three-port-to-Two-Port Noise Transformations*

A three-port network is converted to a two-port when one of the three ports is terminated with a load as feedback. The four noise parameters $\{F_{min}, R_n, \Gamma_{opt}\}$ given by two-port circuit simulations of the resultant two-port are dependent on the three-port noise matrix and the feedback. Shown in Figure 3-9 is a three-port network of which the third port is terminated with an admittance of $Y_3 = G_3 + j \cdot B_3$, having a thermal noise represented by i_{G3} where $\overline{|i_{G3}|^2} = 4kT\Delta f \cdot G_3$.

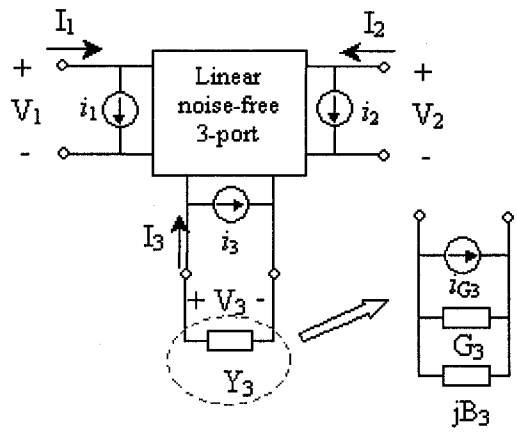

Figure 3-9. Conversion of a three-port to a two-port network with feedback.

Applying Kirchhoff's rules to the third port leads to

$$-I_3 = Y_3 V_3 + i_{G3} \tag{3-19}$$

Substituting (3-18) into (3-16) leads to

$$\begin{aligned}\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} &= \begin{pmatrix} Y_{11} - \frac{Y_{13}Y_{31}}{Y_4} & Y_{12} - \frac{Y_{13}Y_{32}}{Y_4} \\ Y_{21} - \frac{Y_{23}Y_{31}}{Y_4} & Y_{22} - \frac{Y_{23}Y_{32}}{Y_4} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} i_1 - \frac{Y_{13}}{Y_4}(i_3 + i_{G3}) \\ i_2 - \frac{Y_{23}}{Y_4}(i_3 + i_{G3}) \end{pmatrix} \\ &= \begin{pmatrix} Y_{11}' & Y_{12}' \\ Y_{21}' & Y_{22}' \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} i_1' \\ i_2' \end{pmatrix}\end{aligned} \tag{3-20}$$

where $Y_4 = Y_{33} + Y_3$ and $(Y)'$ is the Y matrix of the resultant two-port while i_1' and i_2' are the corresponding equivalent noise current sources.

When the third port is shorted, i.e. Y_3 is infinity, as a special case of feedback, (3-19) can be simplified into

$$\begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-21}$$

Noise analysis of the resultant two-port will involve only i_1 and i_2. Therefore, the generated four noise parameters $\{F_{min}, R_n, \Gamma_{opt}\}$ from a corresponding two-port circuit simulation can be converted to $\{\overline{|i_1|^2}, \overline{|i_2|^2}, \overline{i_1 i_2^*}\}$. By shorting each of the three ports respectively, a three-port noise matrix can be de-embedded from three sets of two-port circuit simulations.

The noise model of a resultant two-port in Figure 3-9 is shown in Figure 3-10 [3.4]. Its four noisy poles are denoted as the noise voltage source u', the uncorrelated noise current source i_n', and the correlation admittance Y'_{cor}, where $\overline{|u'|^2} = 4kT\Delta f \cdot R'_n$ and $\overline{|i'_n|^2} = 4kT\Delta f \cdot G'_n$.

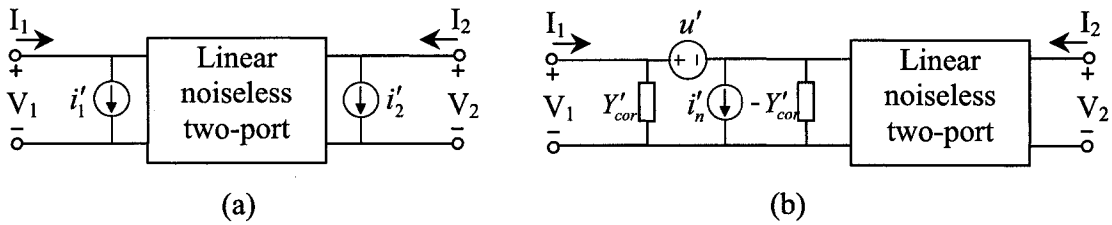

Figure 3-10. (a) Equivalent two-port network of Figure 3-9 with external noise currents i_1' and i_2'; (b) Equivalent two-port network with input-referred noise four poles.

The relation between the four noisy poles and the equivalent noise currents i_1' and i_2' is given as [3.4]

$$\begin{pmatrix} i_1' \\ i_2' \end{pmatrix} = \begin{pmatrix} Y'_{cor} - Y'_{11} & 1 \\ -Y'_{21} & 0 \end{pmatrix} \begin{pmatrix} u' \\ i'_n \end{pmatrix} \tag{3-22}$$

Combining (3-20) and (3-22) gives

$$\begin{pmatrix} Y'_{cor} - Y'_{11} & 1 \\ -Y'_{21} & 0 \end{pmatrix} \begin{pmatrix} u' \\ i'_n \end{pmatrix} = \begin{pmatrix} 1 & 0 & -\frac{Y_{13}}{Y_4} \\ 0 & 1 & -\frac{Y_{23}}{Y_4} \end{pmatrix} \begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} - \begin{pmatrix} \frac{Y_{13}}{Y_4} \\ \frac{Y_{23}}{Y_4} \end{pmatrix} (i_{G3}) \tag{3-23}$$

The independency between u' and i'_n leads to

$$\overline{u' \cdot i_n'^{*}} = 0 \tag{3-24}$$

The independency between i_{G3} and i_1, i_2, i_3 leads to

$$\overline{i_{G3} \cdot i_1^{*}} = 0,\ \overline{i_{G3} \cdot i_2^{*}} = 0,\ \overline{i_{G3} \cdot i_3^{*}} = 0 \tag{3-25}$$

Substitution of u' and i_n' resulting from (3-23) into (3-24) gives

$$Y'_{cor} = Y'_{11} - Y'_{21} \cdot \frac{\overline{i_1 i_2^{*}} - \frac{Y_{13}}{Y_4}\overline{i_2^{*} i_3} - \frac{Y_{23}^{*}}{Y_4^{*}}\overline{i_1 i_3^{*}} + \frac{Y_{13}Y_{23}^{*}}{|Y_4|^2}\left(\overline{|i_3|^2} + \overline{|i_{G3}|^2}\right)}{\overline{|i_2|^2} + \left|\frac{Y_{23}}{Y_4}\right|^2\left(\overline{|i_3|^2} + \overline{|i_{G3}|^2}\right) - \frac{Y_{23}^{*}}{Y_4^{*}}\overline{i_2 i_3^{*}} - \frac{Y_{23}}{Y_4}\overline{i_2^{*} i_3}} \tag{3-26}$$

Multiplication of (3-23) by its conjugate gives

$$\overline{|u'|^2} = \frac{1}{|Y'_{21}|^2}\left[\overline{|i_2|^2} + \frac{|Y_{23}|^2}{|Y_4|^2}\left(\overline{|i_3|^2} + \overline{|i_{G3}|^2}\right) - \frac{Y_{23}^{*}}{Y_4^{*}}\overline{i_2 i_3^{*}} - \frac{Y_{23}}{Y_4}\overline{i_2^{*} i_3}\right] \tag{3-27}$$

$$\begin{aligned}\overline{|i_n'|^2} = &\left[\overline{|i_1|^2} + \frac{|Y_{13}|^2}{|Y_4|^2}\left(\overline{|i_3|^2} + \overline{|i_{G3}|^2}\right) - \frac{Y_{13}^{*}}{Y_4^{*}}\overline{i_1 i_3^{*}} - \frac{Y_{13}}{Y_4}\overline{i_1^{*} i_3}\right] \\ &- \frac{|Y'_{cor} - Y'_{11}|^2}{|Y'_{21}|^2}\left[\overline{|i_2|^2} + \frac{|Y_{23}|^2}{|Y_4|^2}\left(\overline{|i_3|^2} + \overline{|i_{G3}|^2}\right) - \frac{Y_{23}^{*}}{Y_4^{*}}\overline{i_2 i_3^{*}} - \frac{Y_{23}}{Y_4}\overline{i_2^{*} i_3}\right]\end{aligned} \tag{3-28}$$

The dependency of two-port noise parameters, $\{\overline{|u'|^2},\ \overline{|i_n'|^2},\ Y'_{cor}\}$ on the nine entities $\{\overline{|i_1|^2},\ \overline{|i_2|^2},\ \overline{|i_3|^2},\ \overline{i_1 i_2^{*}},\ \overline{i_1 i_3^{*}},\ \overline{i_2 i_3^{*}}\}$ of a three-port noise current matrix is explained in (3-25)-(3-27). Conversion from $\{\overline{|u'|^2},\ \overline{|i_n'|^2},\ Y'_{cor}\}$ to $\{F_{min}, R_n, \Gamma_{opt}\}$ can be readily done using equations given before.

3.4 Example of Three-Port Noise Analysis

An N-MOSFET from a standard CMOS 0.18-μm technology is used as an example. The three-port scattering matrix S_{3P} is extracted at a frequency of 5.3-GHz with L_s = 0 with

schematic configuration shown in Figure 3-11. The three-port noise current matrix $\mathbf{N}_{3P}$ is extracted using the procedure discussed above. The two-port scattering matrix $\mathbf{S}_{2P}$ and noise current matrix $\mathbf{N}_{2P}$ are also extracted with port 3 grounded and $L_s = 0$. The scattering matrix can be converted to a Y matrix using equations in [3.8]. The matrices are listed below as

$$\mathbf{S}_{3P} = \begin{pmatrix} 0.945\angle -37.0^\circ & 0.199\angle 58.1^\circ & 0.274\angle 56.8^\circ \\ 1.024\angle 136.8^\circ & 0.828\angle -47.8^\circ & 1.162\angle -35.1^\circ \\ 0.997\angle -19.1^\circ & 0.163\angle 49.3^\circ & 0.384\angle 167.6^\circ \end{pmatrix}$$

$$\mathbf{N}_{3P} = \begin{pmatrix} 1.34 & 4.35\angle 85.7^\circ & 4.36\angle -84.6^\circ \\ 4.35\angle -85.7^\circ & 480 & 465\angle 174.0^\circ \\ 4.36\angle 84.6^\circ & 465\angle -174.0^\circ & 488 \end{pmatrix} * 1e-4$$

$$\mathbf{S}_{2P} = \begin{pmatrix} 0.874\angle -64.2^\circ & 0.152\angle 40.5^\circ \\ 2.83\angle 124.9^\circ & 0.698\angle -68.3^\circ \end{pmatrix}$$

$$\mathbf{N}_{2P} = \begin{pmatrix} 1.34 & 4.35\angle 85.7^\circ \\ 4.35\angle -85.7^\circ & 480 \end{pmatrix} * 1e-4$$

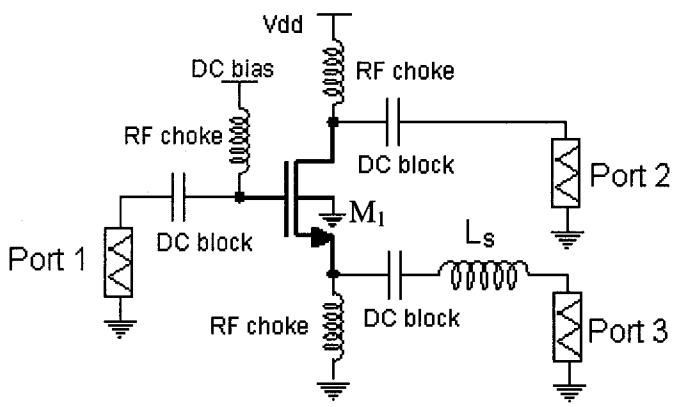

Figure 3-11. Extraction configuration of the three-port scattering and noise matrices.

Changes of the noise parameters $\{F_{min}, R_n, \Gamma_{opt}\}$ of the N-MOSFET, with L_s varying from 0 to 5-nH, are predicted using both the presented three-port theory with $\mathbf{S}_{3P}$ and $\mathbf{N}_{3P}$ and

the two-port theories in [3.1, 3.2, 3.3] with $\mathbf{S}_{2P}$ and $\mathbf{N}_{2P}$. The computation results are compared to the results of two-port circuit simulations with parametric analysis of L_s.

From the comparison in Figure 3-11, 12, 13, it can be seen that the noise parameters predicted by both the three-port and the two-port approaches start at the same points as the simulation results when L_s is zero. As L_s increases, predications by the three-port theory accurately follow the simulation results while the two-port theory gives inaccurate predications. Therefore, it is necessary to use the three-port noise theory with three-port noise matrix to predict the change of the noise parameters with respect to source feedback for a three-terminal MOSFET.

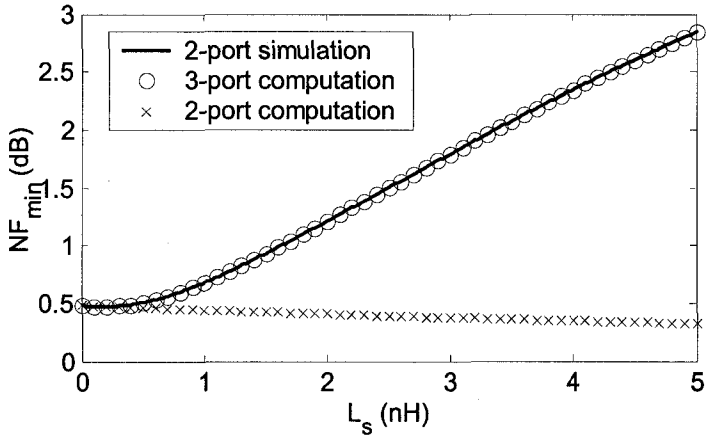

Figure 3-12. Simulated and computed NF_{min} versus L_s.

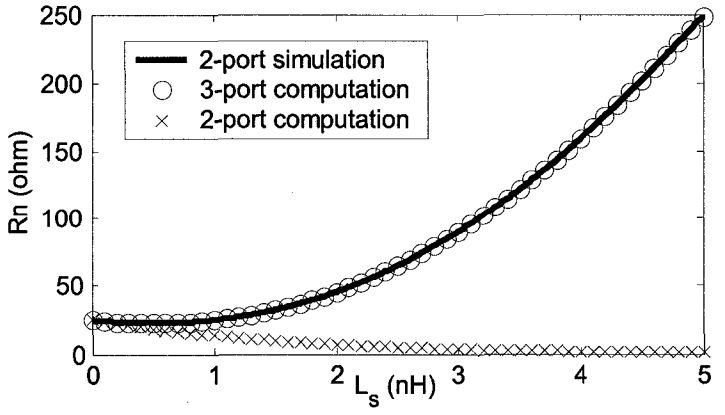

Figure 3-13. Simulated and computed R_n versus L_s.

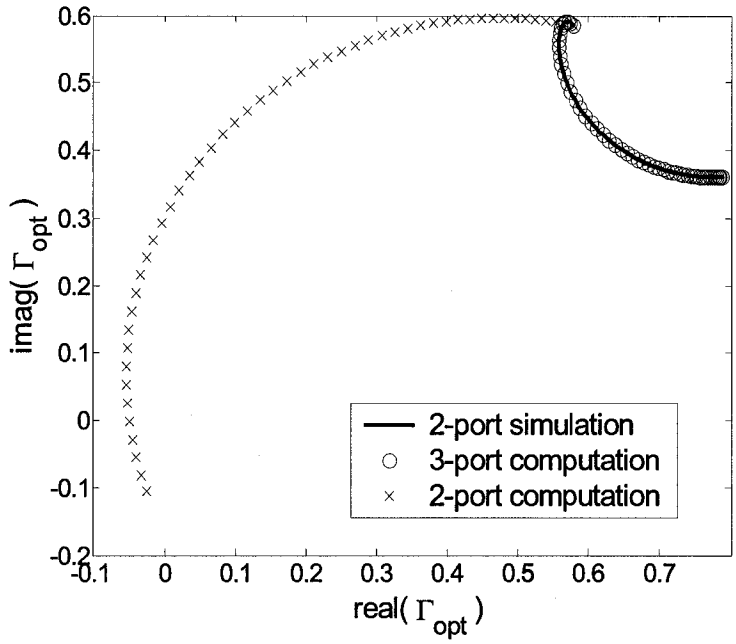

Figure 3-14. Simulated and computed Γ_{opt} versus L_s.

3.5 Application of Three-Port Noise Analysis

The present noise transformation is used in the design of an LNA to optimize series feedback for simultaneous noise and power match. Shown in Figure 3-15 is a single-ended LNA with series feedback L_s and L_a. L_{in} and C_{in}, L_{out} and C_{out} consist of input and output matching networks respectively. The three-port S matrix and noise matrix of the transistor M_1 are given in the previous section. The two-port S matrix and noise matrix of the transistor M_2 at a frequency of 5.3 GHz with source and drain as port 1 and 2 respectively and gate grounded are listed below as

$$\mathbf{S}_{2P}^{M2} = \begin{pmatrix} 0.442\angle -172.8^\circ & 0.0492\angle 19.3^\circ \\ 1.25\angle -26.3^\circ & 0.873\angle -36.8^\circ \end{pmatrix}$$

$$\mathbf{N}_{2P}^{M2} = \begin{pmatrix} 4.35e-2 & 4.19e-2\angle -175.9^\circ \\ 4.19e-2\angle 175.9^\circ & 4.31e-2 \end{pmatrix}$$

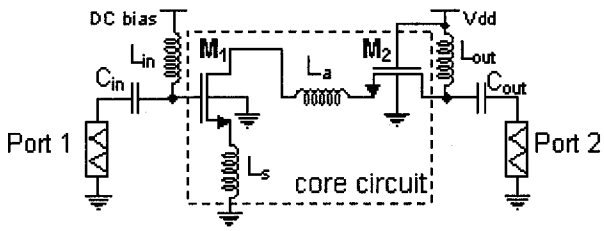

Figure 3-15. Schematic of single-ended LNA with feedback.

The simultaneous conjugate match points of the core circuit are denoted as $\Gamma_{in,SCM}$, $\Gamma_{out,SCM}$ for source and load respectively. $\Gamma_{in,SCM}$, $\Gamma_{out,SCM}$, and Γ_{opt} of the core circuit are all dependent on L_s and L_a. Tuning of L_s and L_a can satisfy various gain and noise requirements. Computation using the three-port theory finds a combination of L_s = 0.74 nH and L_a = 0.43 nH that yields an equal value of 0.544+j·0.473 for both Γ_{opt} and $\Gamma_{in,SCM}$. This means simultaneous noise and power match can be realized under this condition. The corresponding matching networks are 2.00 nH, 0.285 pF, 2.54 nH, 0.159 pF for L_{in}, C_{in}, L_{out}, C_{out} respectively. The scattering parameters **S** and noise figure are plotted in Figure 3-16 and Figure 3-17. It can be seen that at a frequency of 5.3 GHz the gain is maximized to 17.1 dB while the noise figure is minimized to 1.06 dB.

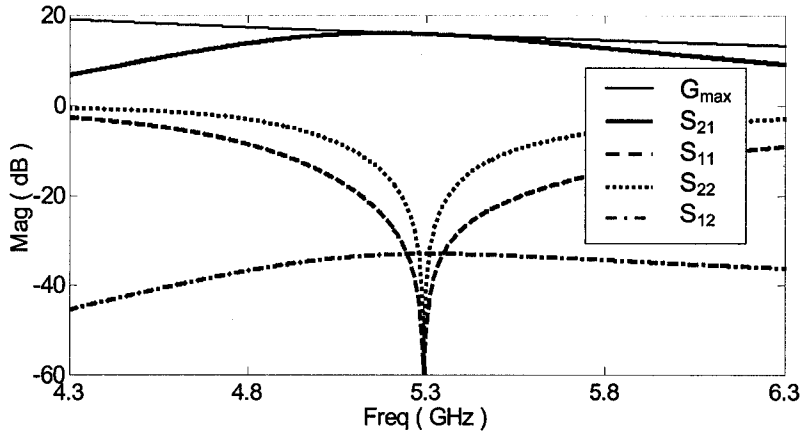

Figure 3-16. Simulated S parameters.

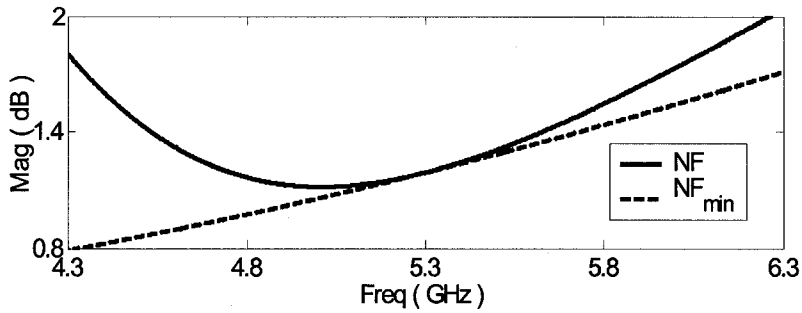

Figure 3-17. Simulated NF and NF_{min}.

3.6 Multi-Port Noise Analysis

3.6.1 *Multi-Port Noise Analysis*

The three-port noise analysis can be extended to the case of a multi-port network with several ports terminated with feedback so that optimization of multiple feedback can be realized. For an N-port network shown in Figure 3-18, the internal noise sources are modeled with external noise current sources i_1, i_2, …, i_N since a Y matrix is used. The analytical relations between the voltages and currents can be written as

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_{N-k} \\ I_{N-k+1} \\ \vdots \\ I_N \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & \cdots & Y_{1,N-k} & Y_{1,N-k+1} & \cdots & Y_{1,N} \\ Y_{21} & Y_{22} & \cdots & Y_{2,N-k} & Y_{2,N-k+1} & \cdots & Y_{2,N} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{N-k,1} & Y_{N-k,2} & \cdots & Y_{N-k,N-k} & Y_{N-k,N-k+1} & \cdots & Y_{N-k,N} \\ Y_{N-k+1,1} & Y_{N-k+1,2} & \cdots & Y_{N-k+1,N-k} & Y_{N-k+1,N-k+1} & \cdots & Y_{N-k+1,N} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ Y_{N,1} & Y_{N,2} & \cdots & Y_{N,N-k} & Y_{N,N-k+1} & \cdots & Y_{N,N} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \\ V_{N-k+1} \\ \vdots \\ V_N \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \\ i_{N-k+1} \\ \vdots \\ i_N \end{pmatrix} \tag{3-29}$$

Assume k ports out of N ports of this network are terminated with admittances $Y_m = G_m + j \cdot B_m$, having thermal noise sources represented by i_m^G where $\overline{\left|i_m^G\right|^2} = 4kT\Delta f \cdot G_m$ and m = N-k+1, N-k+2, …, N. The equivalent circuit is shown in Figure 3-19.

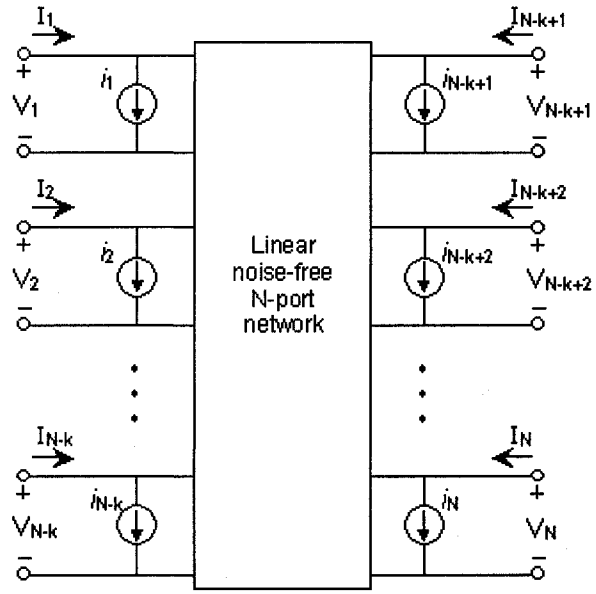

Figure 3-18. An equivalent representation of a linear noisy N-port network with internal noise sources.

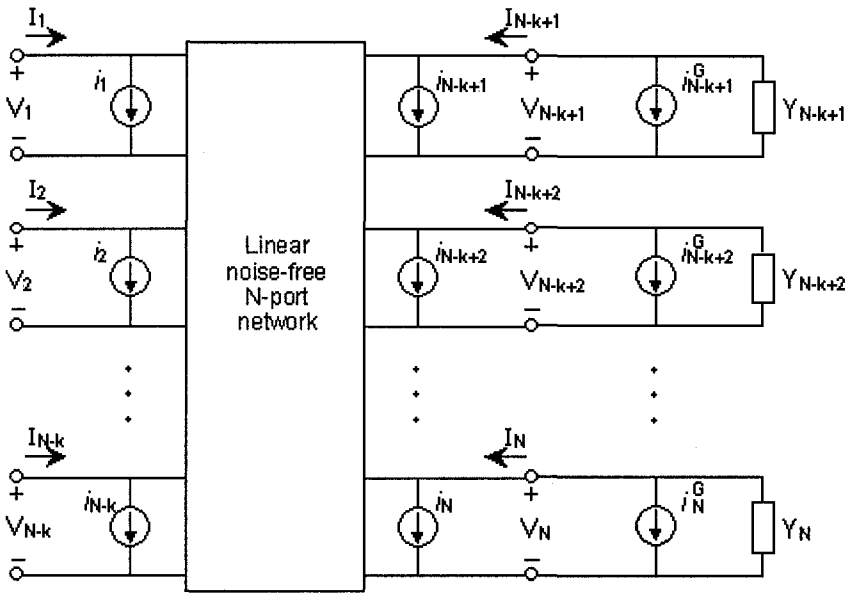

Figure 3-19. A linear noisy N-port network terminated with multiple feedback.

Applying Kirchhoff's rules to the N-k+1th to Nth port leads to

$$\begin{pmatrix} I_{N-k+1} \\ I_{N-k+2} \\ \vdots \\ I_N \end{pmatrix} = -\begin{pmatrix} Y_{N-k+1} & 0 & \cdots & 0 \\ 0 & Y_{N-k+2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Y_N \end{pmatrix}\begin{pmatrix} V_{N-k+1} \\ V_{N-k+2} \\ \vdots \\ V_N \end{pmatrix} - \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix} \tag{3-30}$$

Define (Y_A), (Y_B), (Y_C), (Y_D) and (Y_T) as

$$(Y_A) = \begin{pmatrix} Y_{11} & Y_{12} & \cdots & Y_{1,N-k} \\ Y_{21} & Y_{22} & \cdots & Y_{2,N-k} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N-k,1} & Y_{N-k,2} & \cdots & Y_{N-k,N-k} \end{pmatrix} \tag{3-31}$$

$$(Y_B) = \begin{pmatrix} Y_{1,N-k+1} & Y_{1,N-k+2} & \cdots & Y_{1,N} \\ Y_{2,N-k+1} & Y_{2,N-k+2} & \cdots & Y_{2,N} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N,N-k+1} & Y_{N,N-k+2} & \cdots & Y_{N,N} \end{pmatrix} \tag{3-32}$$

$$(Y_C)=\begin{pmatrix} Y_{N-k+1,1} & Y_{N-k+1,2} & \cdots & Y_{N-k+1,N-k} \\ Y_{N-k+2,1} & Y_{N-k+2,2} & \cdots & Y_{N-k+2,N-k} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N,1} & Y_{N,2} & \cdots & Y_{N,N-k} \end{pmatrix} \tag{3-33}$$

$$(Y_D)=\begin{pmatrix} Y_{N-k+1,N-k+1} & Y_{N-k+1,N-k+2} & \cdots & Y_{N-k+1,N} \\ Y_{N-k+2,N-k+1} & Y_{N-k+2,N-k+2} & \cdots & Y_{N-k+2,N} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{N,N-k+1} & Y_{N,N-k+2} & \cdots & Y_{N,N} \end{pmatrix} \tag{3-34}$$

$$(Y_T)=\begin{pmatrix} Y_{N-k+1} & 0 & \cdots & 0 \\ 0 & Y_{N-k+2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & Y_N \end{pmatrix} \tag{3-35}$$

(3-29) and (3-30) can be rewritten respectively as

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_{N-k} \\ I_{N-k+1} \\ \vdots \\ I_N \end{pmatrix} = \begin{pmatrix} Y_A & Y_B \\ Y_C & Y_D \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \\ V_{N-k+1} \\ \vdots \\ V_N \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \\ i_{N-k+1} \\ \vdots \\ i_N \end{pmatrix} \tag{3-36}$$

$$\begin{pmatrix} I_{N-k+1} \\ I_{N-k+2} \\ \vdots \\ I_N \end{pmatrix} = -(Y_T) \begin{pmatrix} V_{N-k+1} \\ V_{N-k+2} \\ \vdots \\ V_N \end{pmatrix} - \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix} \tag{3-37}$$

(3-36) can be decomposed into two equations as

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_{N-k} \end{pmatrix} = (Y_A) \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \end{pmatrix} + (Y_B) \begin{pmatrix} V_{N-k+1} \\ V_{N-k+2} \\ \vdots \\ V_N \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \end{pmatrix} \tag{3-38}$$

$$\begin{pmatrix} I_{N-k+1} \\ I_{N-k+2} \\ \vdots \\ I_N \end{pmatrix} = (Y_C)\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \end{pmatrix} + (Y_D)\begin{pmatrix} V_{N-k+1} \\ V_{N-k+2} \\ \vdots \\ V_N \end{pmatrix} + \begin{pmatrix} i_{N-k+1} \\ i_{N-K+2} \\ \vdots \\ i_N \end{pmatrix} \tag{3-39}$$

Combing of (3-37) and (3-39) leads to

$$\begin{pmatrix} V_{N-k+1} \\ V_{N-k+2} \\ \vdots \\ V_N \end{pmatrix} = -(Y_D + Y_T)^{-1}\left[(Y_C)\cdot\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \end{pmatrix} + \begin{pmatrix} i_{N-k+1} \\ i_{N-K+2} \\ \vdots \\ i_N \end{pmatrix} + \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix}\right] \tag{3-40}$$

Substituting (3-40) into (3-38) leads to

$$\begin{aligned} \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_{N-k} \end{pmatrix} &= \left[(Y_A) - (Y_B)(Y_D + Y_T)^{-1}(Y_C)\right]\cdot\begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_{N-k} \end{pmatrix} \\ &+ \left\{\begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \end{pmatrix} - (Y_B)(Y_D + Y_T)^{-1}\left[\begin{pmatrix} i_{N-k+1} \\ i_{N-K+2} \\ \vdots \\ i_N \end{pmatrix} + \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix}\right]\right\} \end{aligned} \tag{3-41}$$

The linear and noise behavior of the resultant (N-k)-port network is characterized by (3-41). The equivalent model of the (N-k)-port network is shown in Figure 3-20, where the corresponding noise current sources are denoted as i_1', i_2', ..., i_{N-k}'. The analytical relation between the (N-k) noise current sources and the original N noise current sources is given by

$$\begin{pmatrix} i_1' \\ i_2' \\ \vdots \\ i_{N-k}' \end{pmatrix} = \left\{\begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \end{pmatrix} - (Y_B)\cdot(Y_D + Y_T)^{-1}\cdot\left[\begin{pmatrix} i_{N-k+1} \\ i_{N-K+2} \\ \vdots \\ i_N \end{pmatrix} + \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix}\right]\right\} \tag{3-42}$$

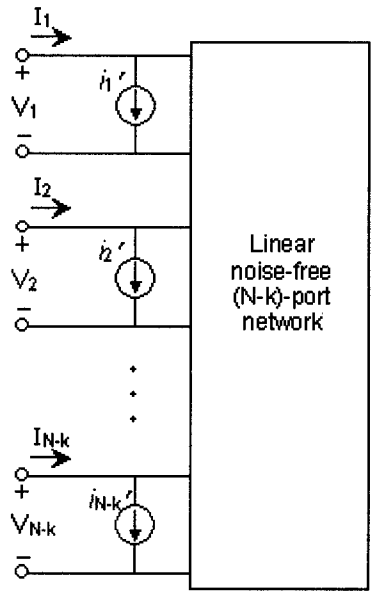

Figure 3-20. Equivalent circuit of the (N-k)-port network with external noise current sources.

Define $\mathbf{i}_0$, $\mathbf{i}_1$, $\mathbf{i}_2$, $\mathbf{i}_G$ respectively as

$$\mathbf{i}_0 = \begin{pmatrix} i_1' \\ i_2' \\ \vdots \\ i_{N-k}' \end{pmatrix} \tag{3-43}$$

$$\mathbf{i}_1 = \begin{pmatrix} i_1 \\ i_2 \\ \vdots \\ i_{N-k} \end{pmatrix} \tag{3-44}$$

$$\mathbf{i}_2 = \begin{pmatrix} i_{N-k+1} \\ i_{N-K+2} \\ \vdots \\ i_N \end{pmatrix} \tag{3-45}$$

$$\mathbf{i}_G = \begin{pmatrix} i^G_{N-k+1} \\ i^G_{N-k+2} \\ \vdots \\ i^G_N \end{pmatrix} \tag{3-46}$$

(3-42) can be rewritten as

$$\mathbf{i}_0 = \mathbf{i}_1 - (Y_B)\cdot(Y_D + Y_T)^{-1}\cdot(\mathbf{i}_2 + \mathbf{i}_G) \tag{3-47}$$

Applying a Hermitian transformation to (3-47) leads to

$$\mathbf{i}_0^{\mathrm{H}} = \left[\mathbf{i}_1 - (Y_B)\cdot(Y_D + Y_T)^{-1}\cdot(\mathbf{i}_2 + \mathbf{i}_G)\right]^{\mathrm{H}} \tag{3-48}$$

The noise current matrix of the resultant (N-k)-port network is given by the time average of the multiplication of (3-47) and (3-48) as

$$\overline{\mathbf{i}_0\cdot\mathbf{i}_0^{\mathrm{H}}} = \overline{\left[\mathbf{i}_1 - (Y_B)(Y_D + Y_T)^{-1}(\mathbf{i}_2 + \mathbf{i}_G)\right]\cdot\left[\mathbf{i}_1 - (Y_B)(Y_D + Y_T)^{-1}(\mathbf{i}_2 + \mathbf{i}_G)\right]^{\mathrm{H}}} \tag{3-49}$$

Because $\mathbf{i}_G$ is independent of $\mathbf{i}_1$, $\mathbf{i}_2$, (3-49) can be simplified into:

$$\begin{aligned} \overline{\mathbf{i}_0\cdot\mathbf{i}_0^{\mathrm{H}}} = {} & \overline{\mathbf{i}_1\cdot\mathbf{i}_1^{\mathrm{H}}} - (Y_B)\cdot(Y_D + Y_T)^{-1}\cdot\overline{\mathbf{i}_2\cdot\mathbf{i}_1^{\mathrm{H}}} \\ & - \overline{\mathbf{i}_1\cdot\mathbf{i}_2^{\mathrm{H}}}\cdot\left(Y_D{}^{\mathrm{H}} + Y_T{}^{\mathrm{H}}\right)^{-1}\cdot(Y_B)^{\mathrm{H}} \\ & + (Y_B)\cdot(Y_D + Y_T)^{-1}\cdot\left[\overline{\mathbf{i}_2\cdot\mathbf{i}_2^{\mathrm{H}}} + \overline{\mathbf{i}_G\cdot\mathbf{i}_G^{\mathrm{H}}}\right]\cdot\left(Y_D{}^{\mathrm{H}} + Y_T{}^{\mathrm{H}}\right)^{-1}\cdot(Y_B)^{\mathrm{H}} \end{aligned} \tag{3-50}$$

The noise behavior of the resultant (N-k)-port network can be fully characterized by the noise current matrix given in (3-50). The original N-port noise current matrix can be extracted using the approach discussed in the previous section.

3.6.2 *Four-Port-to-Two-Port Noise Transformation*

A MOSFET should be a four-terminal device if the body terminal is not tied to the substrate. Feedback can be applied in body terminal as well as the source terminal for modification of noise parameters. For the analysis of source and body feedback, a four-port-

to-two-port noise transformation is derived from the multi-port noise analysis. The equations for noise transformation are given below.

The analytical relations between the voltages and currents of a four-port network shown in Figure 3-21 can be written as

$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} + \begin{pmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{pmatrix} \tag{3-51}$$

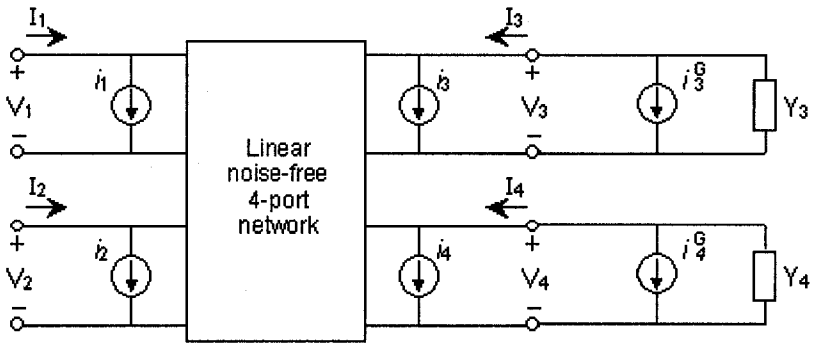

Figure 3-21. A linear noisy 4-port network terminated with multiple feedback.

The four-port noise current matrix is

$$\mathbf{N} = \overline{\mathbf{i}\mathbf{i}^{\mathrm{H}}} = \begin{pmatrix} \overline{i_1 i_1^*} & \overline{i_1 i_2^*} & \overline{i_1 i_3^*} & \overline{i_1 i_4^*} \\ \overline{i_2 i_1^*} & \overline{i_2 i_2^*} & \overline{i_2 i_3^*} & \overline{i_2 i_4^*} \\ \overline{i_3 i_1^*} & \overline{i_3 i_2^*} & \overline{i_3 i_3^*} & \overline{i_3 i_4^*} \\ \overline{i_4 i_1^*} & \overline{i_4 i_2^*} & \overline{i_4 i_3^*} & \overline{i_4 i_4^*} \end{pmatrix} \tag{3-52}$$

(Y_A), (Y_B), (Y_C), (Y_D) and (Y_T) are given respectively as

$$(Y_A) = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \tag{3-53}$$

$$(Y_B) = \begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix} \tag{3-54}$$

$$(Y_C)=\begin{pmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{pmatrix} \tag{3-55}$$

$$(Y_D)=\begin{pmatrix} Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{pmatrix} \tag{3-56}$$

$$(Y_T)=\begin{pmatrix} Y_3 & 0 \\ 0 & Y_4 \end{pmatrix} \tag{3-57}$$

$\mathbf{i}_0$, $\mathbf{i}_1$, $\mathbf{i}_2$, $\mathbf{i}_G$ are given respectively as

$$\mathbf{i}_0 = \begin{pmatrix} i_1' \\ i_2' \end{pmatrix} \tag{3-58}$$

$$\mathbf{i}_1 = \begin{pmatrix} i_1 \\ i_2 \end{pmatrix} \tag{3-59}$$

$$\mathbf{i}_2 = \begin{pmatrix} i_3 \\ i_4 \end{pmatrix} \tag{3-60}$$

$$\mathbf{i}_G = \begin{pmatrix} i_3^G \\ i_4^G \end{pmatrix} \tag{3-61}$$

Substitution of (3-53) – (3-61) into (3-47) leads to

$$\mathbf{i}_0 = \mathbf{i}_1 - \begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix} \cdot \begin{pmatrix} Y_{33}+Y_3 & Y_{34} \\ Y_{43} & Y_{44}+Y_4 \end{pmatrix}^{-1} \cdot (\mathbf{i}_2 + \mathbf{i}_G) \tag{3-62}$$

The noise current matrix of the resultant two-port network can be written as

$$
\begin{aligned}
\mathbf{N}_0 &= \overline{\mathbf{i}_0\mathbf{i}_0^{\mathrm{H}}} \\
&= \overline{\mathbf{i}_1\mathbf{i}_1^{\mathrm{H}}} - \begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix}\begin{pmatrix} Y_{33}+Y_3 & Y_{34} \\ Y_{43} & Y_{44}+Y_4 \end{pmatrix}^{-1} \overline{\mathbf{i}_2\cdot\mathbf{i}_1^{\mathrm{H}}} \\
&\quad - \overline{\mathbf{i}_1\mathbf{i}_2^{\mathrm{H}}}\left[\begin{pmatrix} Y_{33}+Y_3 & Y_{34} \\ Y_{43} & Y_{44}+Y_4 \end{pmatrix}^{-1}\right]^{\mathrm{H}}\begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix}^{\mathrm{H}} \\
&\quad + \begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix}\begin{pmatrix} Y_{33}+Y_3 & Y_{34} \\ Y_{43} & Y_{44}+Y_4 \end{pmatrix}^{-1}\left[\overline{\mathbf{i}_2\mathbf{i}_2^{\mathrm{H}}} + \overline{\mathbf{i}_G\mathbf{i}_G^{\mathrm{H}}}\right] \\
&\qquad \cdot\left[\begin{pmatrix} Y_{33}+Y_3 & Y_{34} \\ Y_{43} & Y_{44}+Y_4 \end{pmatrix}^{-1}\right]^{\mathrm{H}}\begin{pmatrix} Y_{13} & Y_{14} \\ Y_{23} & Y_{24} \end{pmatrix}^{\mathrm{H}}
\end{aligned}
\tag{3-63}
$$

The two-port noise parameters such as $\{R_n, G_n, Y_{cor}\}$ or $\{F_{min}, R_n, \Gamma_{opt}\}$ can be derived from the noise current matrix using (3-10) – (3-13).

3.7 Conclusions

In this chapter, the two-port noise theory has been extended to a three-port noise analysis using a three-port noise current matrix to model the noise behavior of a three-port network. An explicit formulation is given for three-port-to-two-port noise transformation. The approach is applied in the design of a CMOS LNA for simultaneous noise and power match. De-embedding a three-port noise matrix from two-port circuit simulations is also presented.

The three-port noise analysis is generalized to a multi-port noise analysis for the investigation of multiple feedback on multi-port networks. Optimization of noise and power performance of a multi-port circuit with multiple feedback can be achieved using this approach.

The multi-port noise analysis is based on the noise parameters and the Y matrix of a circuit. Therefore, it is independent of semiconductor technology and can be applied to various technologies such as CMOS, SiGe or GaAs active devices.

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CHAPTER 4. DESIGN OF THE LOW-NOISE AMPLIFIER

4.1 Introduction

An LNA is typically the first active stage in a radio receiver. Its performance, such as the noise figure, gains and linearities, is critical to the overall performance of the radio receiver. Previous and recent developments in the design of the LNA have focused on the optimization of the noise figure and input impedance match, which is called simultaneous noise and input match (SNIM) [4.1, 4.2]. However, the transducer gain of an LNA needs to be optimized as well because the noise contribution from stages following the LNA are compressed by this gain. From this point of view, in the design of an LNA, noise measure (M) needs to be optimized as well [4.3]. Noise measure is proportional to the noise figure and inversely proportional to the transducer gain. So a maximum transducer gain with a minimum noise figure will lead to a minimized noise measure. Since the transducer gain of a two-port circuit is dependent on the input and output impedance match, the SNIM optimization technique, which does not consider the output impedance match, does not necessarily lead to the maximum transducer gain although the noise figure is optimized to its minimum. Therefore, these techniques do not necessarily lead to an optimal noise measure.

Recent design approaches have involved tuning of the active device sizes, bias points and feedback, etc, to minimize the noise figure while maintaining the input impedance match. However, the analysis is based on a simplified MOSFET small-signal model that neglects many parasitic components and noise sources. The design strategy heavily relies on

the accuracy of the mathematical model [4.2]. In the design of an LNA for operation in a GHz band, the parasitic components are not negligible so the simplified model is not valid.

This chapter explores the design trade-offs between the transducer gain and the noise figure in the design of a CMOS LNA. An optimization technique with explicit formulas is proposed for optimization of noise and gain match. Because the presented optimization technique is based on the measured noise parameters and S parameters instead of the simplified MOSFET model, this approach is independent of specific device models. Therefore, it is a generic approach that can be applied to other IC technologies such as bipolar transistors. In addition, this approach simplifies the design strategy by not involving sophisticated tuning schemes. The proposed technique is applied in the design of a 5.3-GHz fully integrated LNA in a CMOS 0.18-μm technology.

4.2 Gain Theory for Linear Two-Port Networks

In this section, the gain theory from [4.4] is briefly introduced for a linear two-port network shown in Figure 4-1. The reflection coefficient, Γ, of an admittance, Y, is given by

$$\Gamma = \frac{Y_0 - Y}{Y_0 + Y} \tag{4-1}$$

where Y_0 is the normalization admittance.

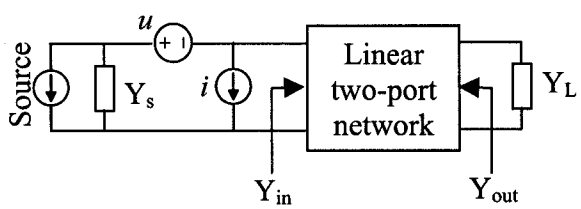

Figure 4-1. An equivalent noise model for a linear noisy two-port circuit.

The input and output admittances of the two-port network are noted as Y_{in} and Y_{out} respectively. The source and load admittances are noted as Y_s and Y_L respectively. Y_{in} is a function of Y_L and Y_{out} is a function of Y_s. Using the reflection coefficients and the S parameters of the two-port network, the analytical relation can be expressed as

$$\Gamma_{in} = \frac{S_{11} - \Delta_S \Gamma_L}{1 - S_{22}\Gamma_L} \tag{4-2}$$

$$\Gamma_{out} = \frac{S_{22} - \Delta_S \Gamma_s}{1 - S_{11}\Gamma_s} \tag{4-3}$$

where

$$\Delta_S = S_{11}S_{22} - S_{12}S_{21} \tag{4-4}$$

The transducer gain G_T of the two-port network is given by

$$G_T = \frac{\left(1 - |\Gamma_s|^2\right) \cdot |S_{21}|^2 \cdot \left(1 - |\Gamma_L|^2\right)}{\left|1 - S_{11}\Gamma_s - S_{22}\Gamma_L + \Delta_S \Gamma_s \Gamma_L\right|^2} \tag{4-5}$$

From (4-5) it can be seen that G_T is dependent on both Γ_s and Γ_L. When the two-port network has a simultaneous conjugate match, which means $\Gamma_s = \Gamma_{in}^*$ and $\Gamma_L = \Gamma_{out}^*$, G_T is optimized to its maximum as

$$G_{T\max} = \left|\frac{S_{21}}{S_{12}}\right|\left(K - \sqrt{K^2 - 1}\right) \tag{4-6}$$

where

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta_S|^2}{2|S_{11}S_{22}|} \tag{4-7}$$

K is named the stability factor of a two-port network. SCM only occurs when K is greater than 1. A two-port network is called unconditionally stable when its K is greater than 1 and Δ_S is less than 1.

4.3 Optimization for Noise and Gain Match

4.3.1 *Simultaneous Noise and Input Impedance Match*

In this section the simultaneous noise and input impedance match (SNIM) technique from [4.5, 4.6] is briefly introduced. N_0 in Figure 4-2 represents a linear two-port network while N_1 and N_2 are ideal lossless impedance matching networks that transform the source and load impedances of 50 Ω to the desired values for optimization of the noise figure and the transducer gain. The cascaded networks of $\{N_1, N_0, N_2\}$, $\{N_1, N_0\}$, $\{N_0, N_2\}$ are noted as M_0, M_1 and M_2 respectively. Y_s', Y_L', Y_{in}', Y_{out}' are the source, load, input and output impedances of N_0 respectively. Γ_s', Γ_L', Γ_{in}', Γ_{out}' are the corresponding reflection coefficients respectively. Y_s, Y_L, Y_{in}, Y_{out} are the source, load, input and output impedances of M_0 respectively. Γ_s, Γ_L, Γ_{in}, Γ_{out} are the corresponding reflection coefficients respectively. The S parameters of the network N_0 and M_0 are denoted as S_{ij} and S_{ij}' respectively.

Since the source and load impedances of M_0 are the normalization impedance (50 Ω), then $\Gamma_{in} = S_{11}'$ and $F_{out} = S_{22}'$. When the input impedance of M_0 is matched, $S_{11}' = 0$. When the output impedance of M_0 is matched, $S_{22}' = 0$. Since N_2 is an ideal lossless network, the two-port noise parameters of M_2 are the same as these of N_0. In addition, the impedance matching levels before and after N_1 or N_2 are preserved, i.e., $|S_{11}|$ of M_2 is equal to $|S_{11}|$ of M_0 and $|S_{22}|$ of M_1 is equal to $|S_{22}|$ of M_0, because of the power conservation.

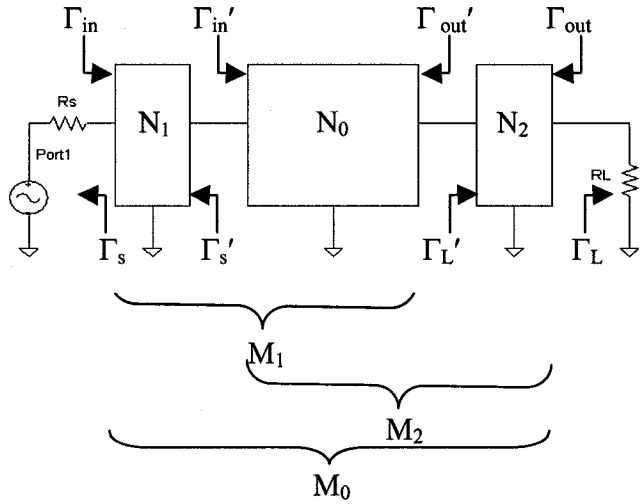

Figure 4-2. A linear two-port network with matching networks for noise and impedance match.

To achieve the minimum noise figure of N_0, the source admittance of N_0, Y_s', needs to be equal to the optimal source admittance of N_0, Y_{opt}, which leads to

$$\Gamma_s' = \Gamma_{opt} \tag{4-8}$$

where Γ_{opt} is the reflection coefficient of Y_{opt}.

To achieve the input impedance match of N_0, the source admittance of N_0, Y_s', needs to be equal to the input impedance of N_0, Y_{in}', which leads to

$$\Gamma_s' = (\Gamma_{in}')^* \tag{4-9}$$

$$|\Gamma_L'| < 1 \tag{4-10}$$

To achieve the simultaneous noise and input impedance match of N_0, Γ_s' has to satisfy both (4-8) and (4-9), which leads to

$$\Gamma_s' = \Gamma_{opt} = (\Gamma_{in}')^* \tag{4-11}$$

The analytical relation between Γ_{in}' and Γ_L' can be expressed using the S parameters as

$$\Gamma'_{in} = \frac{S_{11} - \Delta_S \cdot \Gamma'_L}{1 - S_{22} \cdot \Gamma'_L} \tag{4-12}$$

Substitution of (4-12) into (4-11) leads to

$$\Gamma'_L = \frac{S_{11} + \Gamma_{opt}^*}{\Delta_S - S_{22} \cdot \Gamma_{opt}^*} \tag{4-13}$$

with a constraint imposed by (4-10). The load admittance given by (4-13) is noted as $Y_{L,SNIM}$. The corresponding reflection coefficient is noted as $\Gamma_{L,SNIM}$.

When N_0 is loaded with the optimum source admittance (Y_{opt}) at the input port, and the load impedance ($Y_{L,SNIM}$) given by (4-13) at the output port, the simultaneous noise and input impedance match is realized for this network. However, $Y_{L,SNIM}$ given by (4-13) is not guaranteed to be a positive-real value. Therefore, the solution of (4-10) and (4-13) doesn't always exist.

Substitution of (4-13) into (4-10) gives

$$\left| \Gamma_{opt}^* - \frac{S_{11} - \Delta_S \cdot S_{22}^*}{1 - |S_{22}|^2} \right| < \frac{|S_{12} \cdot S_{21}|}{1 - |S_{22}|^2} \tag{4-14}$$

It is implied by (4-14) that Γ_{opt}^* should lie within a circle to have a valid solution for the load impedance. This circle, which is on the input reflection coefficient plane, maps into the unity circle on the load reflection coefficient plane, and is called the input-referred load stability circle (ILSC). When (4-14) is not satisfied, a valid load impedance cannot be found to achieve SNIM. In this case, lossless series or shunt feedback can be employed to modify the original network of N_0 to change the locations of Γ_{opt}^* and the ILSC.

4.3.2 *Optimization Technique for Noise and Gain Match*

When (4-14) is satisfied, simultaneous noise and input impedance match can be realized by transforming Y_L to $Y_{L,SNIM}$ and Y_s to Y_{opt} respectively. Since the source admittance is fixed to Y_{opt} for minimum noise performance, the output admittance of N_0 is fixed. Generally, Γ_{out}^* is not equal to Γ_L, which means the output impedance of N_0 is not matched to the load impedance. Because the impedance matching level is maintained before and after N_2, the output impedance of M_0 is not matched to its load impedance either. Since the transducer gain is dependent on both the input and the output impedance match, the SNIM technique doesn't necessarily lead to the maximum transducer gain. Furthermore, Γ_{out}^* is significantly different from Γ_L in CMOS technology, which usually leads to a very low level of the output impedance match that dramatically degrades the gain performance. Therefore, the SNIM technique is realized in a way that achieves minimum noise figure performance at the cost of gain performance.

It can be seen from (4-5) that G_T is dependent on S_{11}' and S_{22}'. Under the condition of SCM, $S_{11}' = 0$ and $S_{22}' = 0$, leading to the maximum transducer gain. Under the condition of SNIM, $S_{11}' = 0$ while $S_{22}' \neq 0$ (usually a large number) so that G_T is considerably lower than its maximum. If both S_{11}' and S_{22}' are small numbers, G_T can be optimized close to its maximum. If a small amount of input impedance matching can be used to compensate the output impedance matching, the transducer gain under SNIM can be increased. This design tradeoff can be realized by varying Γ_L' [4.7]. An optimum Γ_L' may be found to maintain both the input and output impedance matching to desired levels. Since the noise parameters of M_2 are independent of the lossless N_2, the noise match will be maintained with a varying Γ_L'.

For a linear two-port network, if the source impedance is fixed, the output impedance is fixed as well. The input and output impedance matching levels are dependent on the load impedance. For a constant impedance matching level at the input or output ports, i.e., $|S_{11}|$ or $|S_{22}|$ is a constant number, the loci of the corresponding load impedances form a circle on the load reflection coefficient plane. This kind of circle will be called the constant input or output matching circle.

The loci of a constant input matching circle lie on various constant output matching circles. There exists a locus that is corresponding to the minimum (thus the best) of the various output matching levels. This locus is the tangent point of the constant input and output matching circles. A set of input and output matching circles are plotted in Figure 4-3.

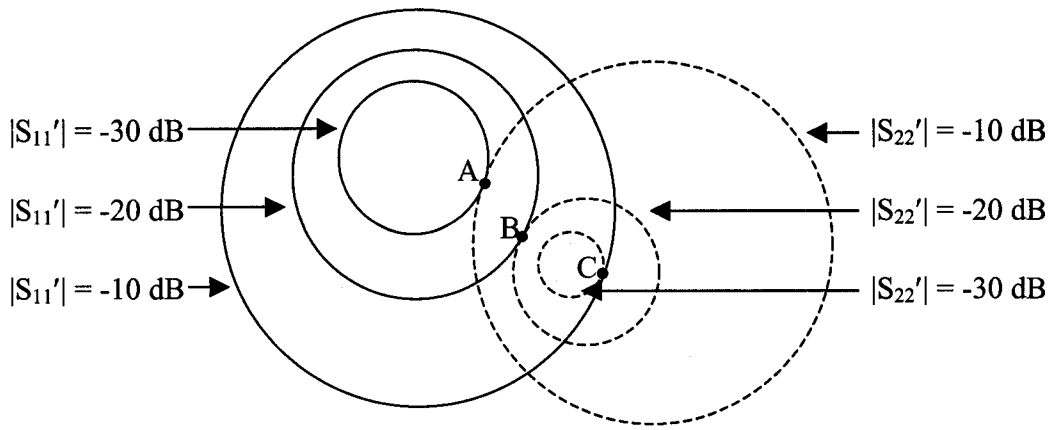

Figure 4-3. Constant input and output matching circles on the load reflection coefficient plane.

As illustrated in Figure 4-3, the constant input matching circle of $|S_{11}'| = -20$ dB on the load reflection coefficient plane is tangent to the constant output matching circle of $|S_{22}| = -20$ dB. Locus B is the tangent point. Its corresponding load impedance gives the best output matching of –20 dB when $|S_{11}'| = -20$ dB. The other loci of the constant input matching

circle of $|S_{11}'| = -20$ dB yield worse output matching levels. It also can be seen that for the input matching of $|S_{11}'| = -30$ dB, the best output matching is $|S_{22}'| = -10$ dB with the load impedance corresponding to the tangent point A. For the input matching of $|S_{11}'| = -10$ dB, the best output matching is $|S_{22}'| = -30$ dB with the load impedance corresponding to the tangent point C.

Therefore, for a given input matching level of n, the best output matching level of m can be found by locating the constant output matching circle tangent to the constant input matching circle of $|S_{11}'| = n$. There are two cases to be considered: outer tangent and inner tangent, as illustrated in Figure 4-4.

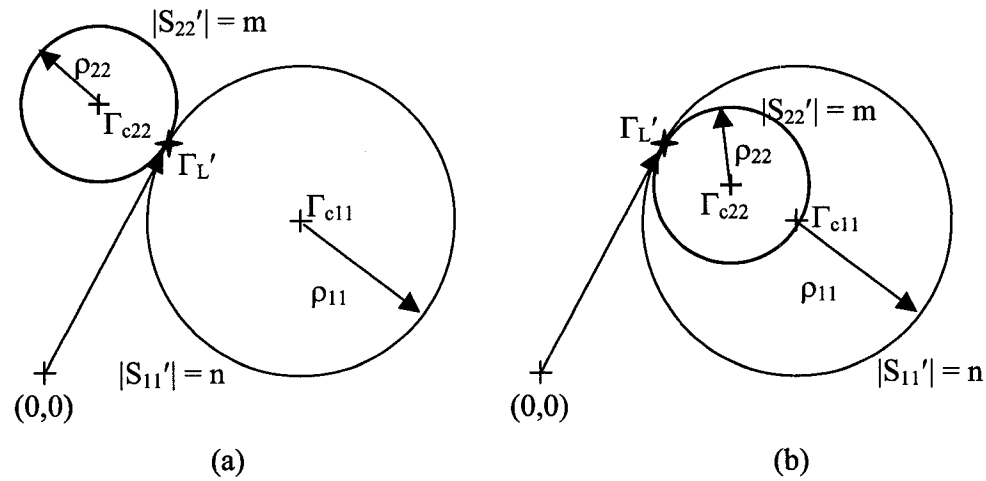

Figure 4-4. Tangent constant input and output matching circles in the load reflection coefficient plane, (a) outer tangent, (b) inner tangent.

For the network shown in Figure 4-2, when $\Gamma_s' = \Gamma_{opt}$, the constant output matching circle of $|S_{22}'| = m$ is given as

$$\left|\Gamma_L' - \Gamma_{c22}\right| = \rho_{22} \tag{4-15}$$

where

$$\Gamma_{c22} = \frac{\Gamma_{L,OZM}(1-m^2)}{1-\left|\Gamma_{L,OZM}\right|^2 m^2} \tag{4-16}$$

$$\rho_{22} = \frac{m\left|1-\left|\Gamma_{L,OZM}\right|^2\right|}{\left|1-\left|\Gamma_{L,OZM}\right|^2 m^2\right|} \tag{4-17}$$

$$\Gamma_{L,OZM} = \left(\Gamma_{out}{}'\right)^*\Big|_{\Gamma_s'=\Gamma_{opt}} = \left(\frac{S_{22}-\Delta_S\cdot\Gamma_{opt}}{1-S_{11}\cdot\Gamma_{opt}}\right)^* \tag{4-18}$$

The constant input matching circle of $|S_{11}'| = n$ is given as:

$$\left|\Gamma_L' - \Gamma_{c11}\right| = \rho_{11} \tag{4-19}$$

where

$$\Gamma_{c11} = -\frac{a^*b - n^2c^*d}{|a|^2 - n^2|c|^2} \tag{4-20}$$

$$\rho_{22} = \frac{m|ad-bc|}{\left||a|^2 - n^2|c|^2\right|} \tag{4-21}$$

$$a = S_{22}\cdot\left(\Gamma_{opt}\right)^* - \Delta_S \tag{4-22}$$

$$b = S_{11} - \left(\Gamma_{opt}\right)^* \tag{4-23}$$

$$c = \Delta_S\cdot\Gamma_{opt} - S_{22} \tag{4-24}$$

$$d = 1 - S_{11}\cdot\Gamma_{opt} \tag{4-25}$$

Usually the input impedance matching is more constrained because it determines how much the input signal power is absorbed into the circuit. With $|S_{11}'| = n$ is specified, the optimum Γ_L' needs to be found that leads to a minimum $|S_{22}'| = m$. As shown in Figure 4-4,

the two constant matching circles of $|S_{11}'| = n$ and $|S_{22}'| = m$ should be tangent to each other. Their center points and radiuses should satisfy

$$|\Gamma_{c22} - \Gamma_{c11}| = \rho_{11} \pm \rho_{22} \tag{4-26}$$

where + sign is for the case of outer tangent and – sign is for the case of inner tangent. Since the center points and radiuses are all functions of m, the minimum output matching level of m can be found by solving (4-26).

Substituting (4-16), (4-17), (4-20) and (4-21) into (4-26) leads to

$$C_4 \cdot m^4 + C_3 \cdot m^3 + C_2 \cdot m^2 + C_1 \cdot m + C_0 = 0 \tag{4-27}$$

where

$$C_4 = |\Gamma_{L,OZM}|^2 (1 - \Gamma_{L,OZM}\Gamma_{c11}^* - \Gamma_{L,OZM}^*\Gamma_{c11} - \rho_{11}^2 |\Gamma_{L,OZM}|^2) + |\Gamma_{c11}|^2 \Gamma_{L,OZM}^4 \tag{4-28}$$

$$C_3 = \pm 2\rho_{11} |\Gamma_{L,OZM}|^2 (1 - |\Gamma_{L,OZM}|^2) \tag{4-29}$$

$$\begin{aligned} C_2 = {} & |\Gamma_{L,OZM}|^2 (2\rho_{11}^2 + \Gamma_{L,OZM}\Gamma_{c11}^* + \Gamma_{L,OZM}^*\Gamma_{c11} - 2|\Gamma_{c11}|^2 - |\Gamma_{L,OZM}|^2) \\ & + \Gamma_{L,OZM}^*\Gamma_{c11} + \Gamma_{L,OZM}\Gamma_{c11}^* - 1 \end{aligned} \tag{4-30}$$

$$C_1 = \mp 2\rho_{11}^2 (1 - |\Gamma_{L,OZM}|^2) \tag{4-31}$$

$$C_0 = |\Gamma_{L,OZM}|^2 - \Gamma_{L,OZM}\Gamma_{c11}^* - \Gamma_{L,OZM}^*\Gamma_{c11} + |\Gamma_{c11}|^2 - \rho_{11}^2 \tag{4-32}$$

There is at most one realistic root out of the four possible roots of (4-27). After m is known, the center point Γ_{c22} and the radius ρ_{c22} of the constant output matching circle of $|S_{22}'| = m$ can be determined using (4-16) and (4-17).

The optimum Γ_L' for the outer tangent case can be found as

$$\Gamma_L' = \frac{\rho_{11}}{\rho_{22} + \rho_{11}} \Gamma_{c22} + \frac{\rho_{22}}{\rho_{22} + \rho_{11}} \Gamma_{c11} \tag{4-33}$$

The optimum Γ_L' for the inner tangent case can be found as

$$\Gamma_L' = \frac{\rho_{11}}{\rho_{11} - \rho_{22}}\Gamma_{c22} + \frac{\rho_{22}}{\rho_{22} - \rho_{11}}\Gamma_{c11} \tag{4-34}$$

The minimum $|S_{22}'|$ = m resulted from (4-27) for a specified $|S_{11}'|$ = n is not guaranteed to meet the design requirement, because there is only one design freedom, Γ_L', but there are two goals, input and output impedance matching, to meet. If $|S_{22}'|$ = m is larger than the required value for a given $|S_{11}'|$ = n, extra design variables such as noiseless feedback can be introduced to modify the network N_0 so that a simultaneous optimum noise match and gain match can be achieved. The introduced feedback will change the noise parameters of the network N_0. Therefore, the multi-port noise analysis presented in the previous chapter should be employed to evaluate the changes due to feedback in the optimization procedure.

4.4 Design of a 5-GHz CMOS LNA

4.4.1 *Schematic View*

The proposed optimization technique is carried out in the design of a fully integrated 5.3-GHz LNA in a wireless communication receiver for IEEE802.11a applications. The schematic of the single-ended LNA is shown in Figure 4-5.

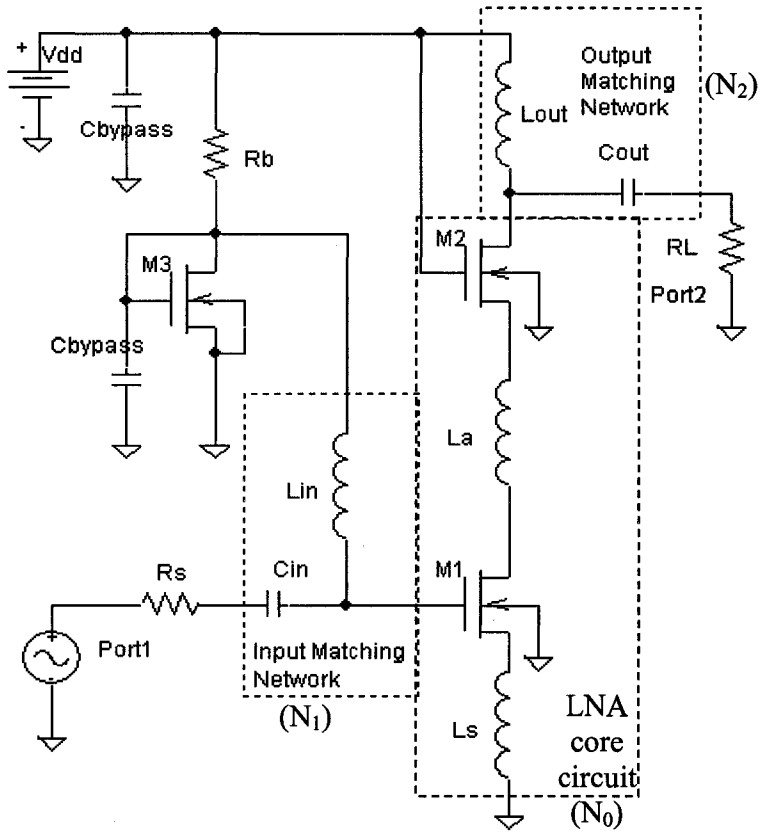

Figure 4-5. Simplified LNA schematic with bias circuitry.

In Figure 4-5, transistors M_1 and M_2 form the LNA core circuit (N_0), a cascaded structure that has a potential of high gain and high isolation. A source degeneration inductor L_s and an inter-stage inductor L_a are series feedback that will be used for optimization of noise and gain match [4.8, 4.9]. The input impedance matching network (N_1) consisting of C_{in} and L_{in} will transform the source impedance of 50 Ω to the optimum source impedance of the LNA core circuit. The output impedance matching network (N_2) consisting of C_{out} and L_{out} will transform the load impedance of 50 Ω to the optimum load impedance that leads to the noise and gain match. C_{in} and C_{out} also serve as the DC blocking capacitors while L_{in} and L_{out} serve as the bias inductors.

4.4.2 *Schematic Design*

S parameters and noise matrices of M_1 and M_2 at a frequency of 5.3 GHz are given in the previous chapter. While $L_s = 0$ and $L_a = 0$, the noise parameters of N_0 are calculated as

$$NF_{min} = 0.759 \text{ dB}, R_n = 28.8\ \Omega, \Gamma_{opt} = 0.543 + j\ 0.574.$$

The S parameters are calculated as

$$(S) = \begin{pmatrix} 0.942 \angle -55.0° & 0.00635 \angle 73.0° \\ 3.00 \angle 111.8° & 0.906 \angle -37.7° \end{pmatrix}$$

The stability factor is less than 1. A shunt 800-Ω resistor at the output port is needed to make the circuit unconditionally stable at this frequency. With this resistor, the noise parameters are transformed to

$$NF_{min} = 0.777 \text{ dB}, R_n = 29.6\ \Omega, \Gamma_{opt} = 0.542 + j\ 0.577$$

The S parameters are transformed to

$$(S) = \begin{pmatrix} 0.942 \angle -55.0° & 0.00602 \angle 73.9° \\ 2.85 \angle 112.7° & 0.810 \angle -38.1° \end{pmatrix}$$

The constant noise circles, the stability circles and Γ_{opt} are plotted in Figure 4-6.

Under this condition, (4-14) is not satisfied so that the SNIM condition doesn't exist. It can be seen from Figure 4-6 as well that Γ_{opt}^* is outside the input-referred load stability circle. It can also be observed that Γ_{opt} is significantly away from $\Gamma_{s,SCM}$, which implies that the impedance matching needs to be compromised a lot to lower the noise figure.

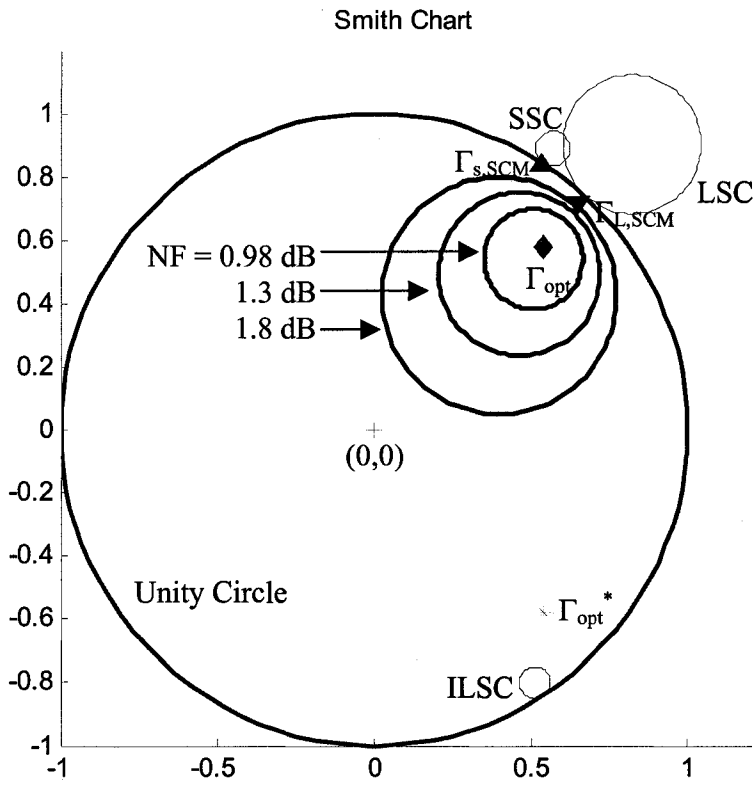

Figure 4-6. Observation of constant noise circles, stability circles, Γ_{opt}, $\Gamma_{s,SCM}$, $\Gamma_{L,SCM}$ on Smith Chart.

Since the circuit is unconditionally stable, the SCM condition exists. If the SCM is realized, the noise figure of the LNA is 4.53 dB, significantly larger than NF_{min} of 0.777 dB. The transducer gain is maximized to 26.0 dB. The noise measure can be calculated to be 1.84.

If noise match is realized at the input port, constant matching circles can be calculated to find optimized gain and matching levels. The input and output constant matching circles are plotted in Figure 4-7.

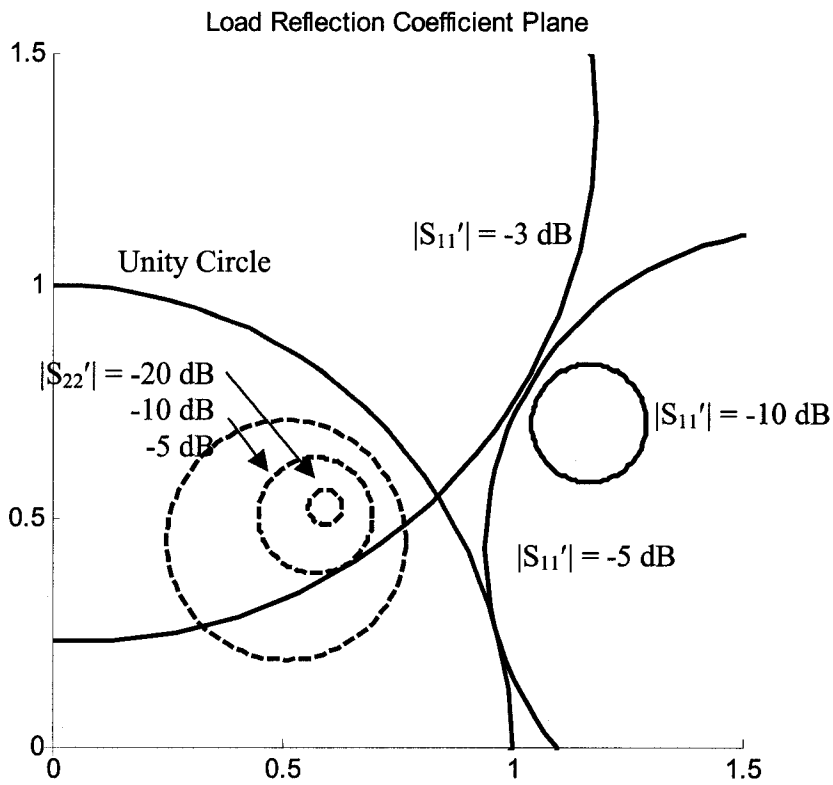

Figure 4-7. Constant matching circles on the load reflection coefficient plane.

It can be observed from Figure 4-7 that the constant input matching circle of $|S_{11}'| = -5$ dB tangent to the unity circle, which implies all the load impedances inside the unity circle lead to input matching levels worse than –5 dB. For the input matching of $|S_{11}| = -3$ dB, the best output matching is $|S_{22}| = -10$ dB, giving a transducer gain of 19.6 dB while the noise figure is maintained at the minimum level. The noise measure can be calculated to be 0.198. However, an input impedance matching of –10 dB is usually required for the LNA design. Therefore this configuration will not be considered.

With observation of the above cases, L_s and L_a are necessary to modify the LNA core circuit for optimization of the noise and gain match.

With $L_s = L_a = 0.6$ nH, the parameters of N_0 are calculated as

$$NF_{min} = 1.02 \text{ dB}, R_n = 28.9\ \Omega, \Gamma_{opt} = 0.535 + j\ 0.506$$

The S parameters are

$$(S) = \begin{pmatrix} 0.760 \angle -43.3° & 0.00685 \angle 83.9° \\ 2.20 \angle 66.0° & 0.899 \angle -37.2° \end{pmatrix}$$

The constant noise circles and the input load stability circle are plotted in Figure 4-8.

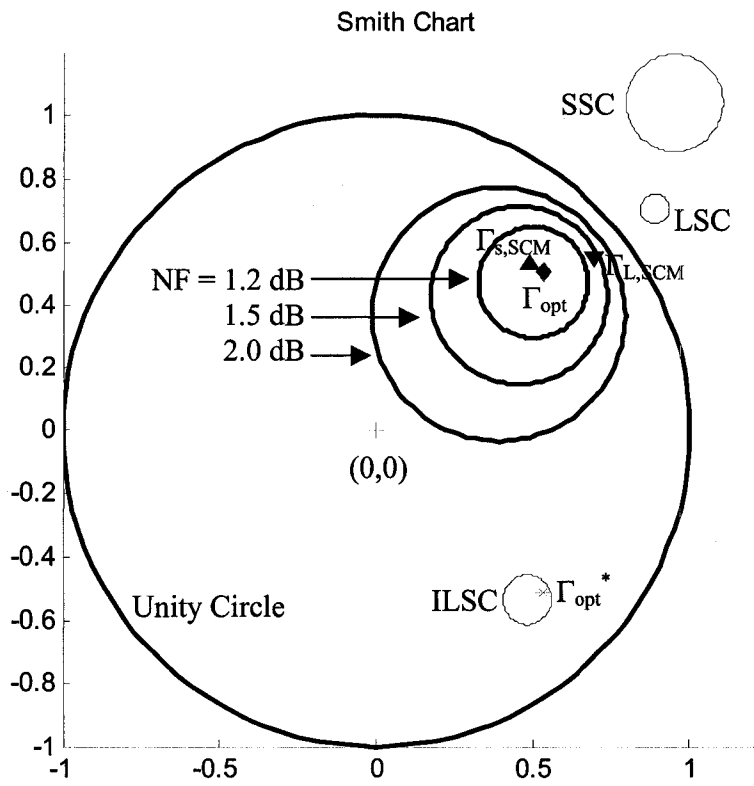

Figure 4-8. Observation of constant noise circles, stability circles, Γ_{opt}, $\Gamma_{s,SCM}$, $\Gamma_{L,SCM}$ on Smith Chart.

It can be observed from Figure 4-6 that the source stability circle (SSC) and the load stability circle (LSC) are out of the unity circle, which means that the circuit is unconditionally stable at this frequency. It can be also seen that Γ_{opt}^* is inside the input load stability circle, which implies the SNIM can be realized. $\Gamma_{s,SCM}$ and $\Gamma_{L,SCM}$ for the SCM

condition are also plotted. It is obvious that $\Gamma_{s,SCM}$ is not equal to Γ_{opt} so that the noise match and the gain match cannot be realized simultaneously. An optimum Γ_L' might exist for an optimum impedance match that leads to a high gain. To achieve the condition of SNIM, Γ_L' = 0.691 + j 0.549 that leads to an output matching of –3.01 dB and a transducer gain of 14.1 dB, 3.1 dB lower than the maximum transducer gain of 17.2 dB.

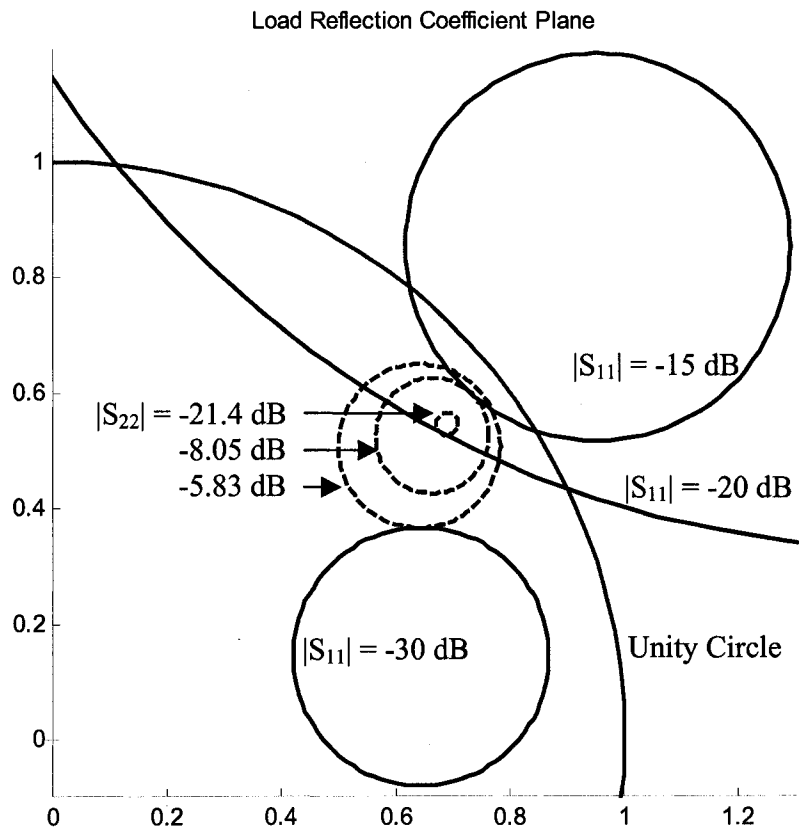

Figure 4-9. Constant matching circles on the load reflection coefficient plane.

To further improve the transducer gain, the constant matching circles with the source admittance fixed to Y_{opt} are plotted on the load reflection coefficient plane. It can be observed that for $|S_{11}'|$ = -30, -20, -15 dB, the best achievable output matching is $|S_{22}'|$ = -5.83 –21.4, -8.05 dB respectively. The corresponding transducer gains are 15.8, 17.1 and 16.4 dB

respectively. The impedance matching of $|S_{11}'|$ = -20 dB and $|S_{22}'|$ = -21.4 dB gives an optimum transducer gain of 17.1 dB, only 0.1 dB lower than its maximum, while the noise figure is maintained at the minimum level. The noise measure is calculated to be 0.270. The corresponding Γ_L' is found to be 0.681 + j 0.531. The passive components of input and output matching networks at 5.3-GHz are: C_{in} = 0.277 pF, L_{in} = 1.96 nH, C_{out} = 0.179 pF, L_{out} = 2.44 nH, which are achievable in CMOS technology.

4.4.3 *Schematic Simulation Results*

The simulation results of S parameters, NF and gains are plotted in Figure 4-10, 4-11 and 4-12 respectively, where it is can be seen that the transducer gain is optimized to the maximum while the noise figure is maintained at the minimum level at the frequency of 5.3-GHz. The performance of the LNA is summarized in Table 4-1.

Table 4-1. Summary of the LNA performance in schematic simulation

Frequency	5.3	GHz
Power Supply	1.5	V
Power Consumption	6.3	mW
Noise Figure	1.0	dB
Transducer Gain	17.1	dB
$\|S_{11}\|$	-20.0	dB
$\|S_{22}\|$	-21.4	dB
IP1dB	-9.5	dBm
IIP3	-1.4	dBm

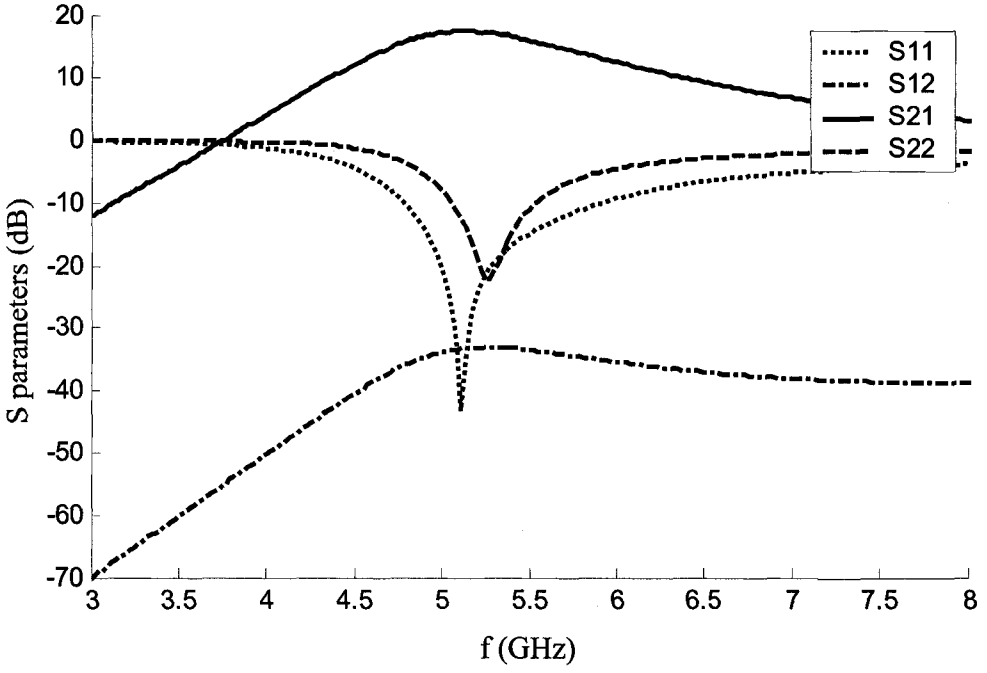

Figure 4-10. S parameters of the LNA with optimized noise and impedance matching.

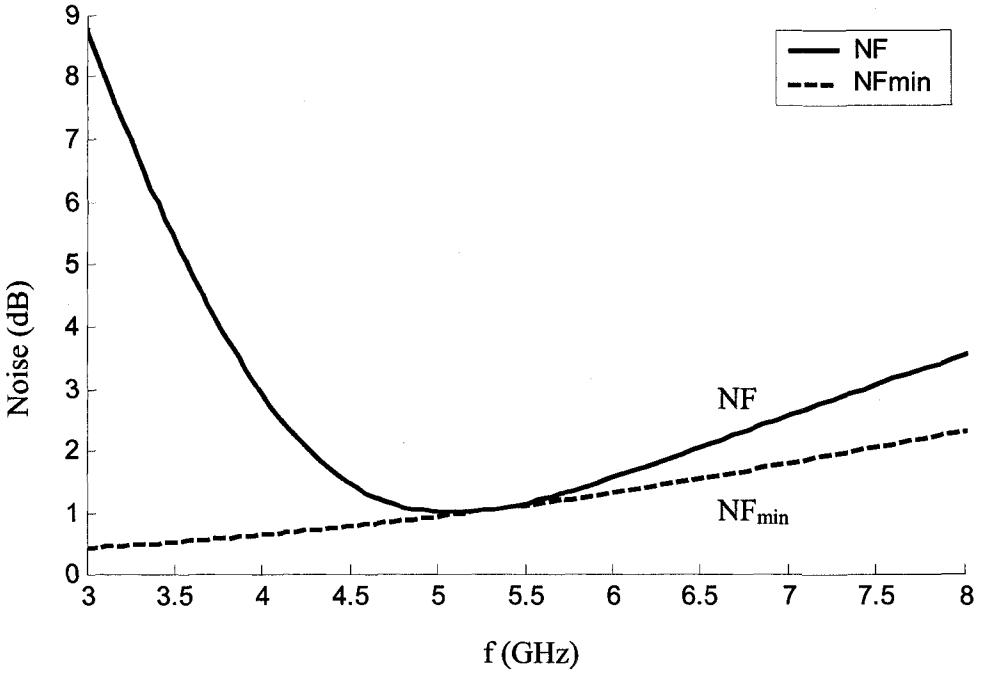

Figure 4-11. NF and NF_{min} of the LNA with optimized noise and impedance match.

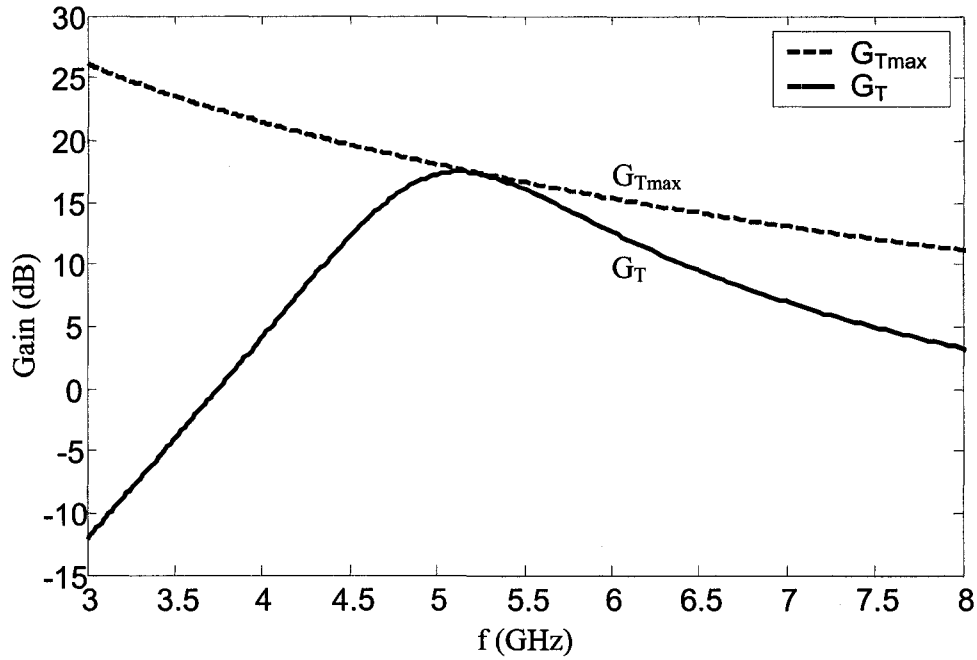

Figure 4-12. G_T and G_{Tmax} of the LNA with optimized noise and impedance match.

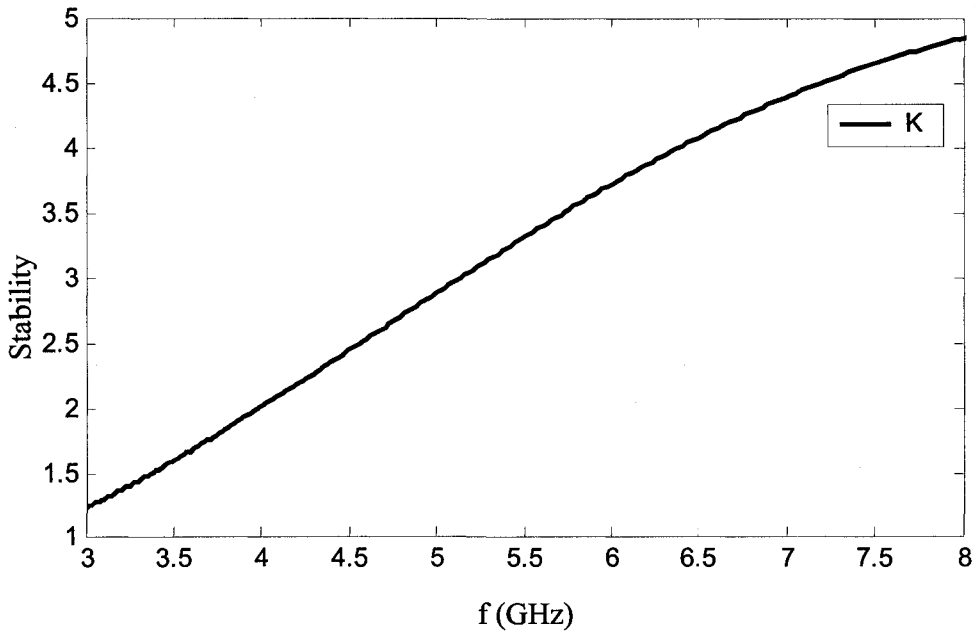

Figure 4-13. Stability factor of the LNA with optimized noise and impedance match.

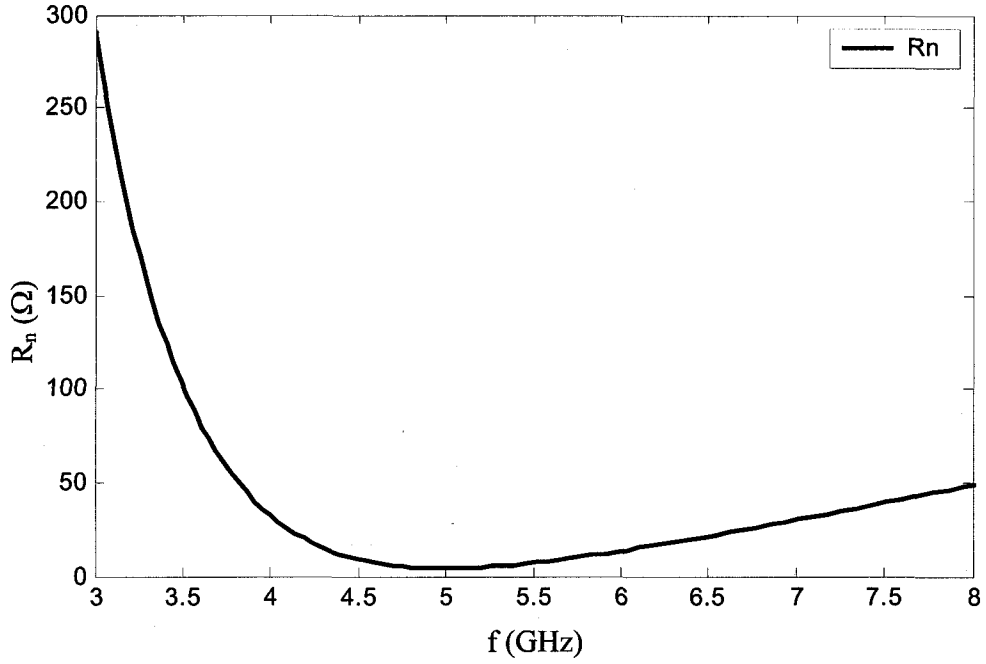

Figure 4-14. R_n of the LNA with optimized noise and impedance match.

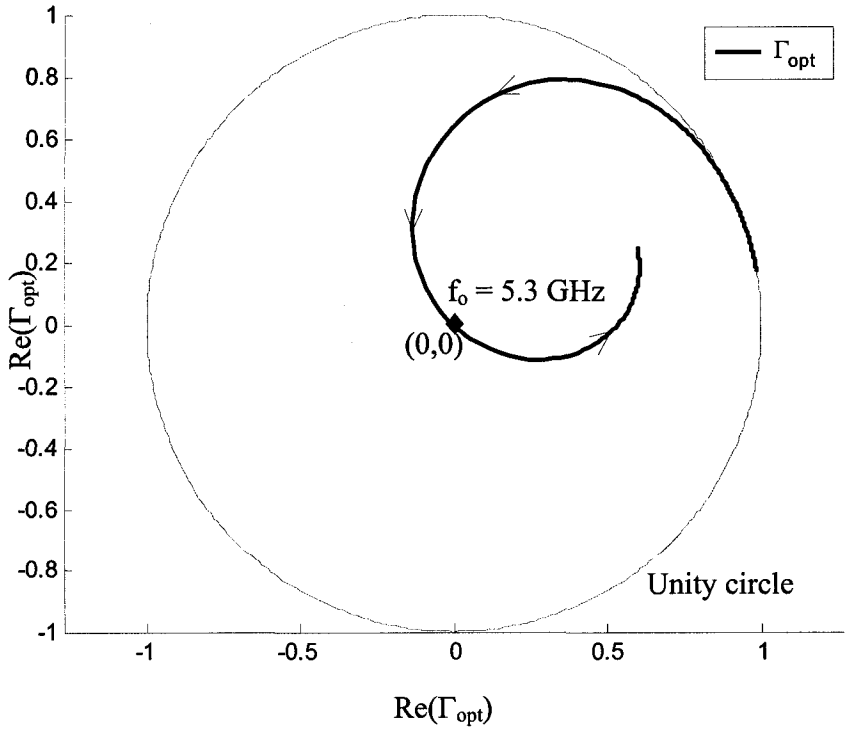

Figure 4-15. Γ_{opt} of the LNA with optimized noise and impedance match.

4.4.4 *Layout View and Post-Layout Simulation Results*

The circuit design is implemented using on-chip capacitors and inductors available in the TSMC 0.18-μm CMOS technology. The layout is shown in Figure 4-16. The post-layout simulation results of S parameters and noise figure are shown in Figure 4-17 and 4-18 respectively.

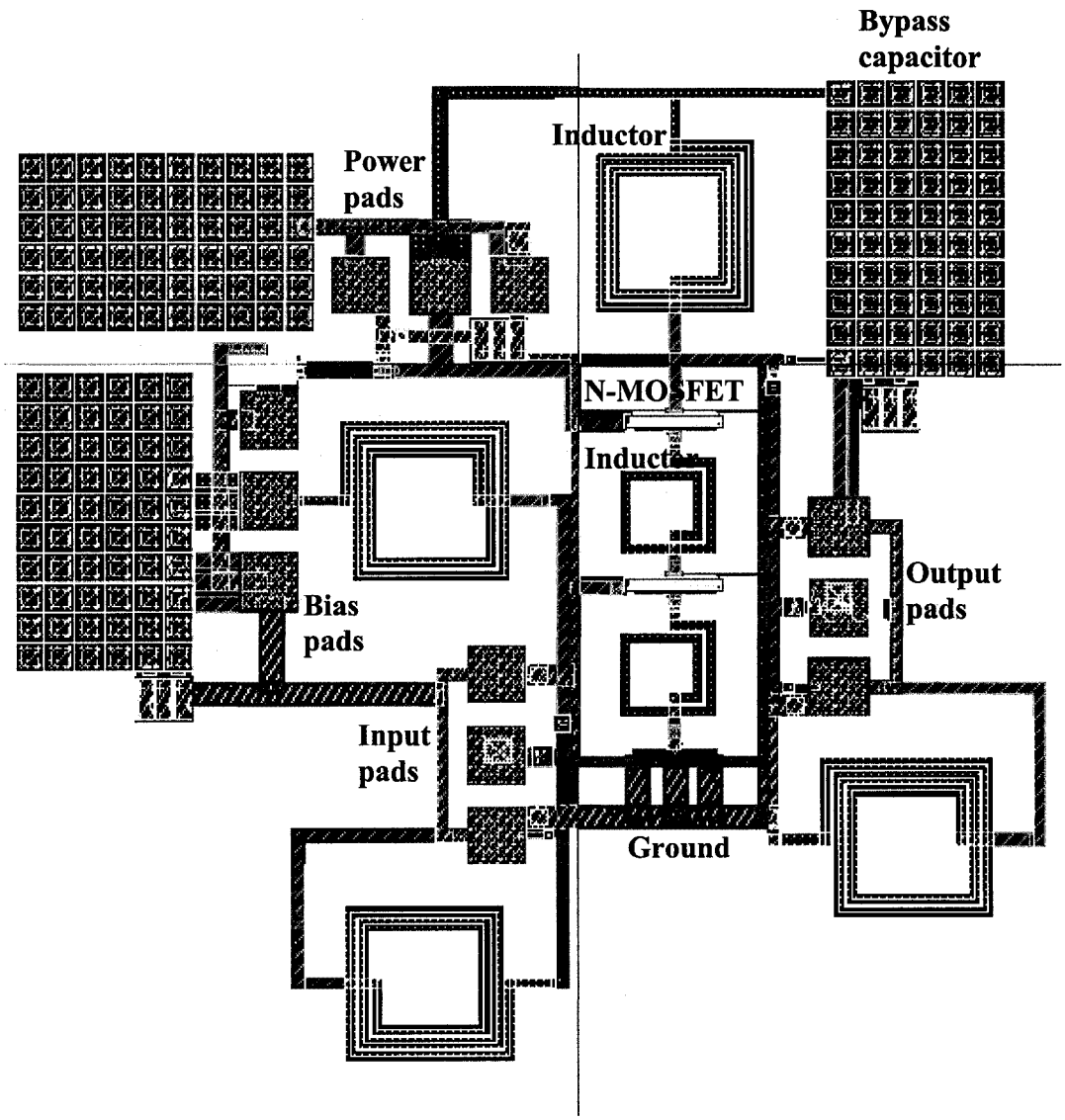

Figure 4-16. Layout view of the LNA in TSMC 0.18-μm CMOS technology.

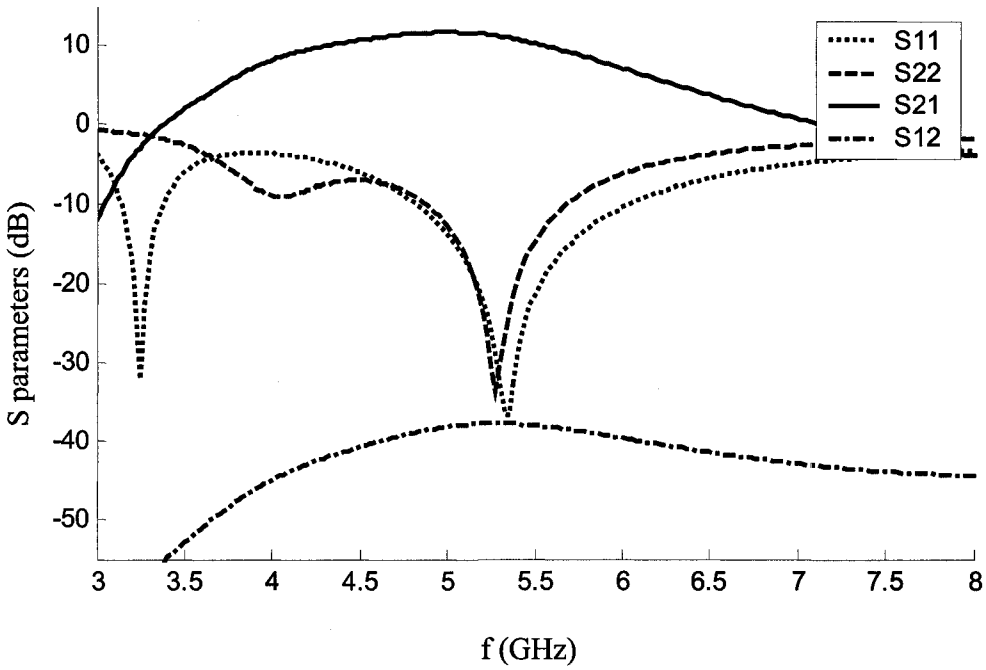

Figure 4-17. Post-layout simulation results: S parameters of the LNA.

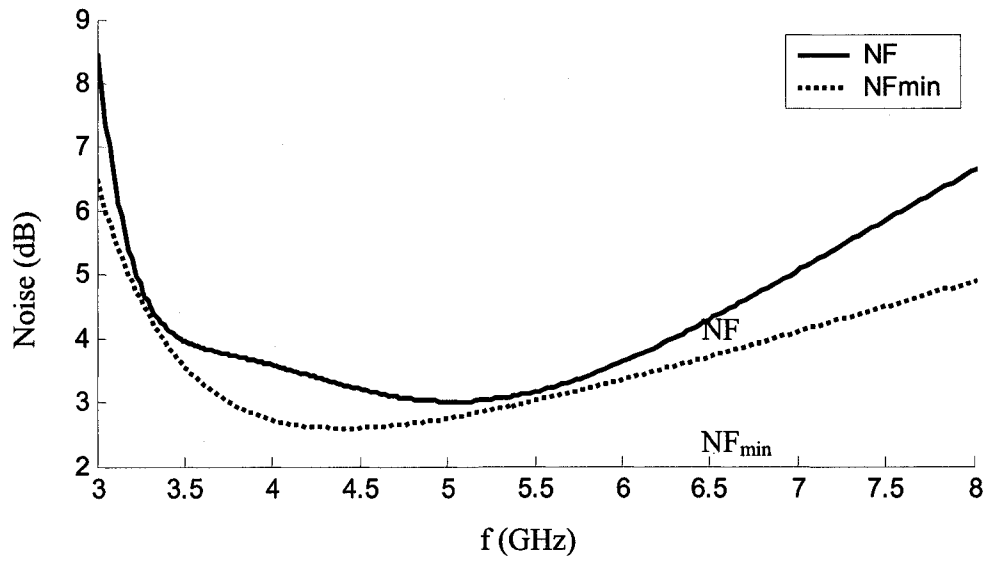

Figure 4-18. Post-layout simulation results: noise figure of the LNA.

4.4.5 *Experiment Measurement*

The chip is fabricated in TSMC 0.18-μm CMOS process on a non-EPI wafer through MOSIS. The die photo is shown in Figure 4-19. Eight chips are measured. The measured S parameters are plotted in Figure 4-20. The S parameters at a frequency of 5.3 GHz of the eight chips are summarized in Table 4-2.

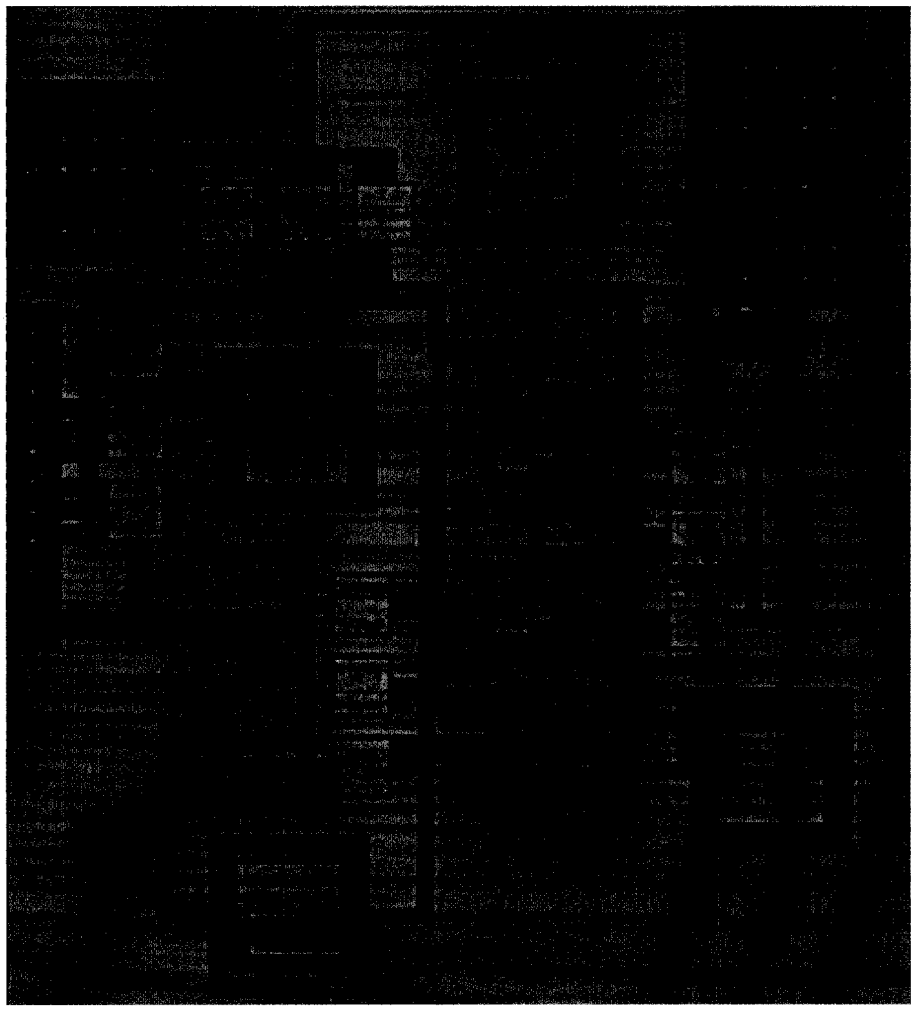

Figure 4-19. Die photo view of the fabricated LNA in a 0.18-μm CMOS technology.

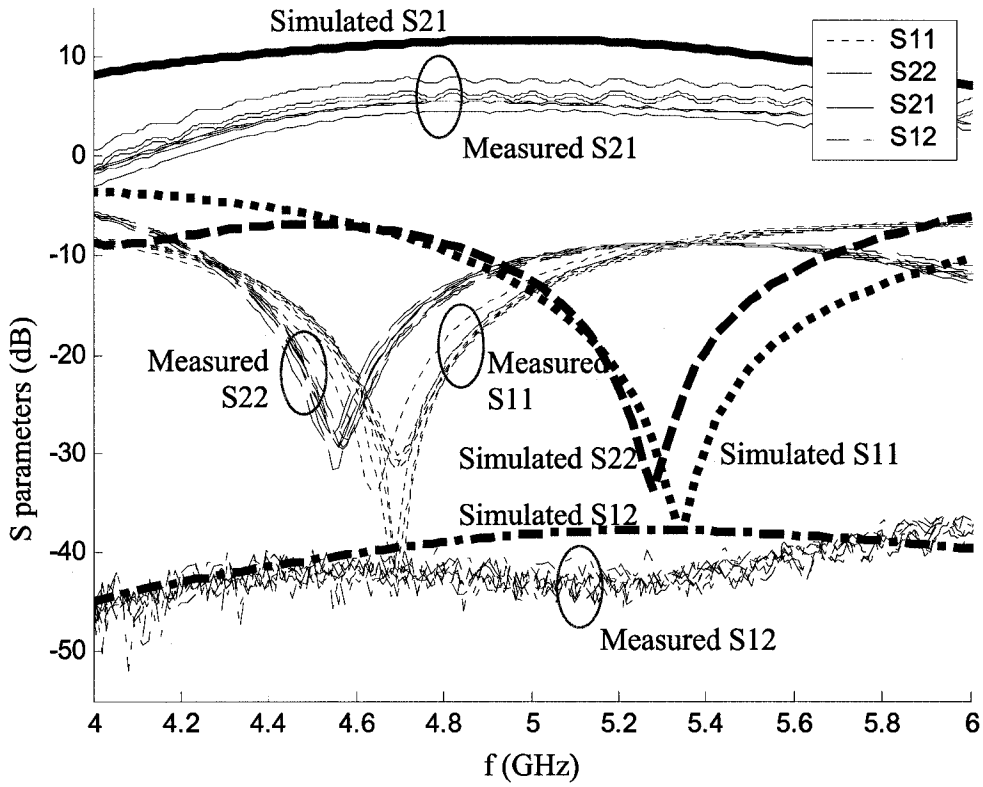

Figure 4-20. Measured S parameters of the LNA versus post-layout simulation results.

Table 4-2. Measured S parameters of eight chips at 5.3 GHz

(dB)	#1	#2	#3	#4	#5	#6	#7	#8	Mean
|S11|	-9.2	-9.1	-8.7	-9.4	-9.3	-9.5	-9.5	-9.7	-9.3
|S22|	-8.9	-8.9	-8.9	-8.9	-8.8	-9.0	-9.0	-8.9	-8.9
|S21|	4.0	4.8	4.7	4.7	4.7	5.9	5.6	7.2	5.2
|S12|	-42.8	-42.4	-42.0	-43.0	-43.0	-43.3	-42.1	-43.8	-42.8

Due to process variation, the impedance matching is shifted to a frequency lower than 5.3 GHz. The average gain at 5.3 GHz is 5.2 dB. The average input and output impedance matching is -9.3 dB and –8.9 dB respectively. The average isolation is –42.8 dB.

The schematic of the LNA is adjusted accordingly to fit the measured data. Extra lossy components are added because the measured gain is lower than the simulation result. The passive components are changed to be larger to account for the frequency shifting. The fitted S parameters are plotted in Figure 4-21.

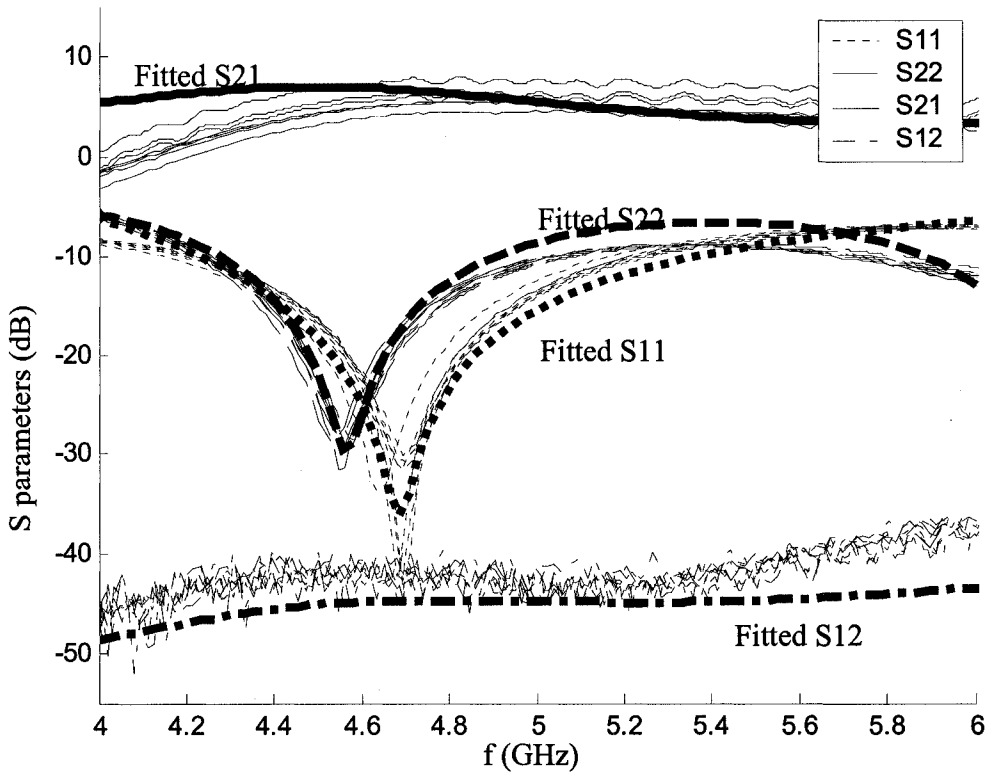

Figure 4-21. Fitted S parameters of the LNA versus measured results.

Due to the lab limitation on noise measurement, the noise performance of the fabricated LNA is estimated from the updated schematic simulation. The estimated noise figure of the corresponding LNA is plotted in Figure 4-22. It can be seen that the noise figure is about 1.7

dB larger than the data from the post-layout simulation because of the extra loss introduced in the circuit to model the lowered gain.

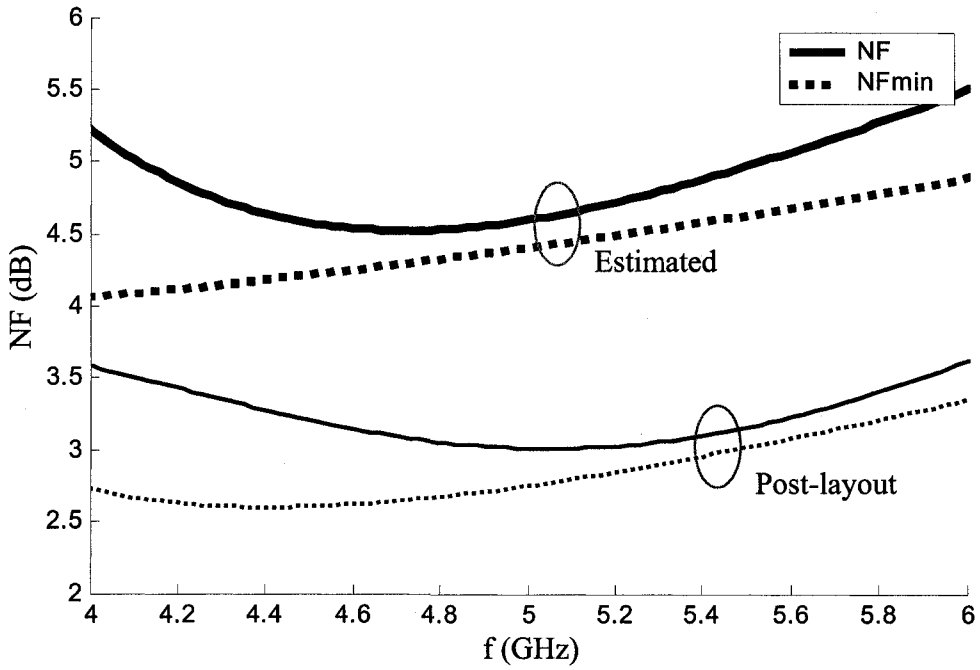

Figure 4-22. Estimated NF of the LNA versus post-layout simulation results.

Table 4-3. Simulated and measured data at 5.3-GHz of the LNA

	Post-layout simulation	Measurement results	
Frequency	5.3	5.3	GHz
Power Supply	1.5	1.5	V
Power Consumption	6.2	6.2	mW
Noise Figure	3.1	4.8 *	dB
Transducer Gain	11.1	5.2	dB
$\|S_{11}\|$	-31.8	-9.3	dB
$\|S_{22}\|$	-30.9	-8.9	dB
IP1dB	-7.2	-2.0	dBm
IIP3	1.3	3.4 *	dBm

* Estimated from updated schematic simulation

4.5 Conclusions

An optimization technique has been presented for optimization of noise and gain match by means of feedback and matching networks. Explicit formulas are given for computing the available impedance matching levels for optimization of the transducer gain while maintaining the minimum noise figure. Feedback tuning might be involved. This optimization technique together with the multi-port noise analysis approach is applied in the design of a 5-GHz LNA in a CMOS 0.18-μm technology.

In on-wafer measurement, the fabricated LNA exhibits an averaged forward gain of 5.2 dB with input and output impedance matching of –9.3 dB and –8.9 dB respectively, and isolation of –42.8 dB. The noise figure is estimated to be 4.8 dB from the updated circuit simulation.

References:

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[4.9] H. S. Kim, X. Li, M. Ismail, "A 2.4GHz CMOS low noise amplifier using an inter-stage matching inductor," *42nd Midwest Symposium on Circuits and Systems*, vol. 2, pp. 1040-1043, 2000.

CHAPTER 5. IMPEDANCE MATCHING NETWORKS

5.1 Introduction

Maximum power transfer, as mentioned in Chapter 4, occurs when the source impedance and the load impedance are conjugate matched to the input impedance and the output impedance respectively. In the transistor amplifier design, it is important to match the source impedance to the input impedance of the transistor to achieve a high power gain. In the design of low-noise amplifiers, it is important to transform the source impedance to the optimum source impedance to achieve minimum noise. The impedance matching can be realized using impedance matching networks. The impedance transformation may be for maximum power transfer, noise performance or other purposes. Impedance matching networks are of two types: narrowband and broadband. In this chapter only the narrowband impedance matching network will be explored because the LNA in this design is desired to be narrowband. Narrowband passive matching networks often consist of two or more reactive components. Based on the configurations formed by the reactive components, they are classified into three kinds: L-section, Π-section and T- section, as shown in Figure 5-1 [5.1]. For an L-section network, the 3-dB bandwidth is not a design parameter since only two components are used [5.1]. For a Π- or a T-section network, it is possible to realize the transformation with control over the bandwidth.

In circuit implementation of the passive matching networks, inductors and capacitors serve as the reactive components. In modern semiconductor technology, the integrated inductors and capacitors will experience different levels of process variation, perturbation

and temperature drift [5.2]. Equipment factors may result in lot-to-lot variation. In general, the on-chip impedance matching networks have to tolerate a large amount of process variation and thus have to be designed carefully to meet the yield requirement.

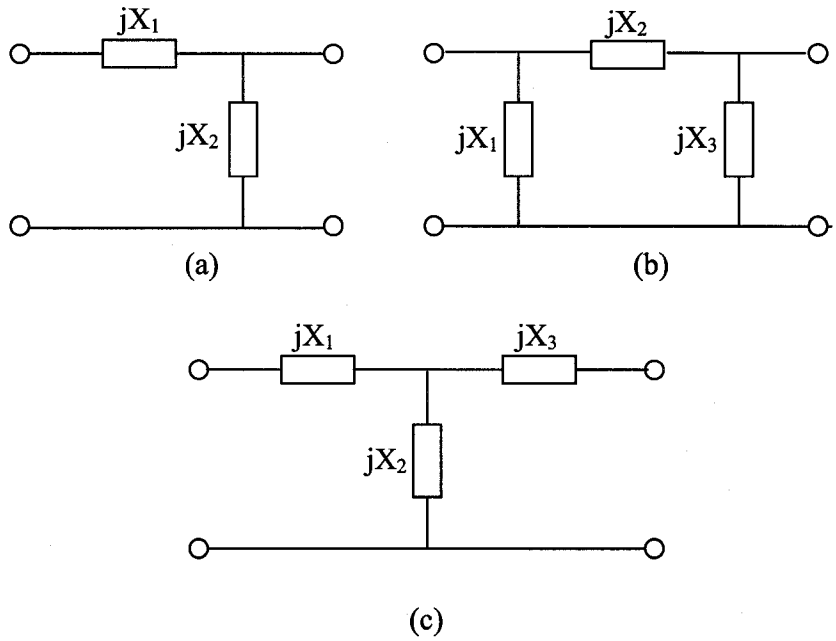


Figure 5-1. Passive impedance matching networks: (a) L-section, (b) Π-section, (c) T-section.

In the current design trend of SOC, many RF building blocks like LNA, mixer, and filters are integrated into one chip. Maintaining impedance matching between cascading stages becomes critical to maximize the power transfer and prevent oscillation.

This chapter focuses on the study of the effect of process variation on several passive impedance matching networks. A process-variation insensitive (PVI) impedance matching network with matched components is presented. With ideally matched passive components, the impedance transformation is nearly immune to process variation. In reality, when passive components are mismatched, the PVI network has a low sensitivity to process variation.

Sensitivity analysis is carried out for the proposed network. Monte Carlo simulation is used to demonstrate the improvement of immunity to process variation as compared to a conventional L-section matching network. This approach can be extended to broadband impedance matching by cascading the proposed network.

5.2 Process-Variation Insensitive Impedance Matching Networks

5.2.1 *Regular Passive Matching Networks*

A positive-real impedance can be transformed to any positive-real impedance by an L-section matching network [5.3]. In an L-section, two pure reactive components, jX_1 and jX_2, are utilized to realize either an upward or a downward transformation as illustrated in Figure 5-2 below. Since the reactive components are ideal, no insertion loss will be experienced in this impedance transformation.

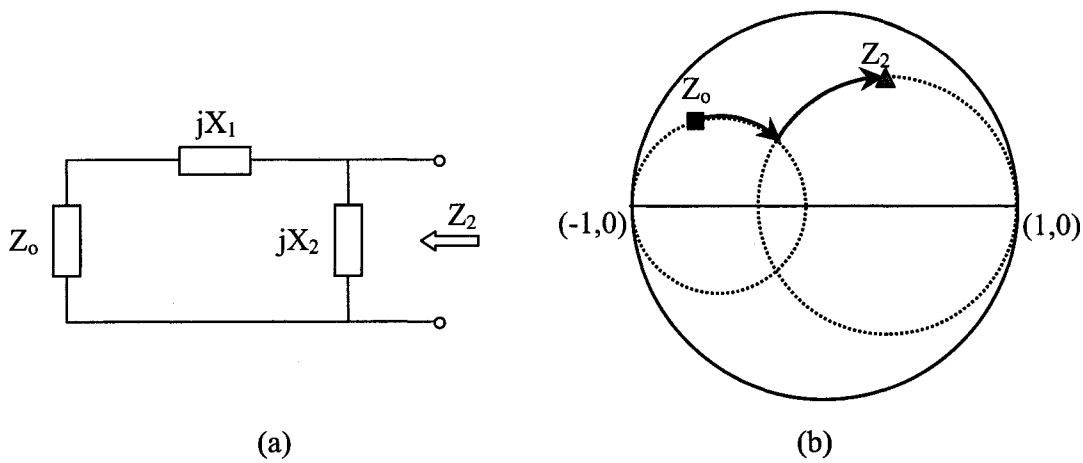


Figure 5-2. An L-section matching network for impedance transformation: (a) L-section structure, (b) illustration of impedance transformation traces on Smith Chart.

Any variation of the passive components in the L-section will cause the impedance transformation to deviate from the desired path, leading to a mismatch between the real and

the desired values. If the transformation is for maximum power transfer, the mismatch will lead to a lower power gain. If the transformation is for the noise match, the mismatch will degrade the noise performance.

If the transformation is realized using the 1-step $1+Q^2$ technique, the two reactive components in an L-section could be an inductor and a capacitor [5.4]. As shown in Figure 5-3, an L-section is used to transform a pure-resistive impedance, R_0, to another pure resistive impedance, R_2.

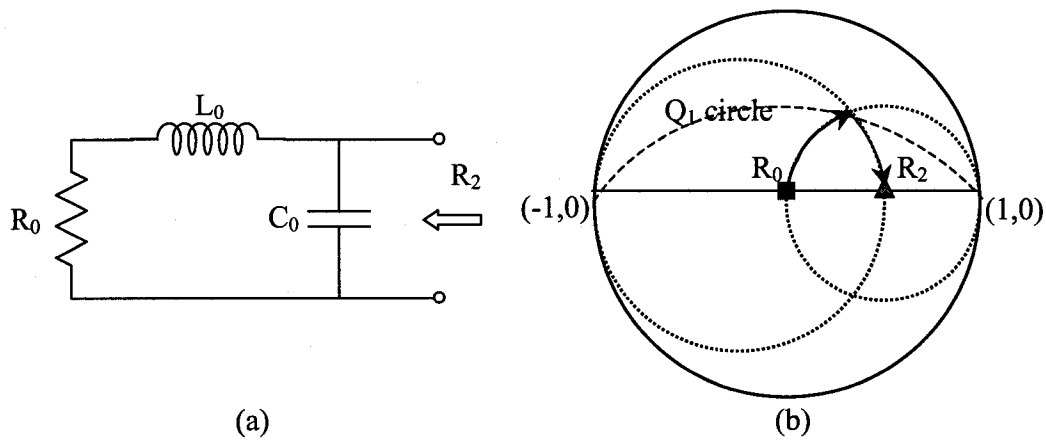


Figure 5-3. (a) 1-step $1+Q^2$matching using an L-section realization with a series capacitor and a shunt inductor, (b) illustration of transformation traces on Smith Chart.

Application of $1+Q^2$ theory in [5.4] leads to

$$R_2 = \frac{R_0 + j\omega L_0}{1-\omega^2 L_0 C_0 + j\omega C_0 R_0} = (1+Q_1^2)\cdot R_0 \tag{5-1}$$

$$\omega L_0 = Q_1 \cdot R_0 \tag{5-2}$$

$$\frac{1}{\omega C_0} = \frac{1+Q_1^2}{Q_1}\cdot R_0 \tag{5-3}$$

Sensitivities of R_2 to the variations of the inductor and the capacitor can be found respectively as

$$S_{L_0}^{R_2} = \frac{\partial R_2}{\partial L_0} \cdot \frac{L_0}{R_2} = \frac{j\omega L_0}{(R_0 + j\omega L_0)(1 - \omega^2 L_0 C_0 + j\omega C_0 R_0)} = \frac{jQ_1(1+Q_1^2)}{(1+jQ_1)^2} \tag{5-4}$$

$$S_{C_0}^{R_2} = \frac{\partial R_2}{\partial C_0} \cdot \frac{C_0}{R_2} = \frac{\omega^2 L_0 C_0 - j\omega C_0 R_0}{1 - \omega^2 L_0 C_0 + j\omega C_0 R_0} = -jQ_1 \tag{5-5}$$

$$\frac{dR_2}{R_2} = S_{C_0}^{R_2} \frac{dC_0}{C_0} + S_{L_0}^{R_2} \frac{dL_0}{L_0} = -j\omega dC_0 R_0 \cdot (1+Q_1^2) + \frac{j\omega dL_0}{R_0} \cdot \frac{1+Q_1^2}{(1+jQ_1)^2} \tag{5-6}$$

Since the process variation mechanisms for on-chip inductors and capacitors are different, the matching performance will be dependent on two independent variables, i.e. variations associated with inductance and capacitance respectively.

5.2.2 *Element of Process-Variation Insensitive Matching Networks*

When an L-section matching network is involved in a circuit design, statistical analysis should be conducted in circuit simulation tools to ensure the circuit performance under process variation meet the design specifications and the yield requirement. Generally the matching network needs to be tuned to satisfy the yield requirement.

As minimum process feature sizes shrink into the sub-micron (nanometer) range, more process variation will be experienced. Capacitance can vary up to ±20% for a metal-insulator-metal (MIM) capacitor [5.2]. It is often the case that process variation will put stringent limits on circuit designs. A significant amount of design effort has been put into the design cycles to meet the yield requirement. Optimization techniques are commonly used to

search for the best solution. When optimization techniques cannot find a solution, introduction of new circuit architectures tolerating process variation is necessary.

In many analog integrated circuit designs, high performance, such as low offset voltage, is achieved with a high degree of precision matching of passive and active devices [5.2]. Similar ideas can be employed in the design of impedance matching networks.

Shown in Figure 5-4(a) is an L-section consisting of two capacitors. At an angular frequency of ω, the shunt capacitor C_1 transforms the source impedance Z_0 to a pure-resistive impedance R_1 while the series capacitor C_2 transforms R_1 to the objective impedance Z_2. The transformation traces on the reflection coefficient plane are plotted in Figure 5-4(b), where it can be seen that Z_0 lies on the constant Q_1 circle and Z_2 lies on the constant Q_2 circle.

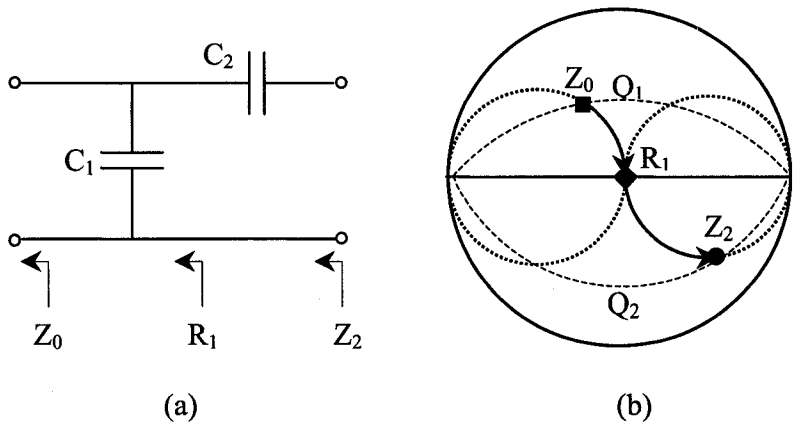


Figure 5-4. (a) An L-section using two capacitors, (b) transformation traces on Smith Chart.

Application of $1+Q^2$ theory in [5.4] leads to

$$Z_2 = Z_0/(1 + j\omega C_1 \cdot Z_0) + 1/(j\omega C_2) \tag{5-7}$$

$$\omega C_1 = Q_1/R_1 \tag{5-8}$$

$$\omega C_2 = 1/(Q_2 \cdot R_1) \tag{5-9}$$

Relations between Z_0, R_1 and Z_2 are governed by

$$Z_0 = R_1/(1 - jQ_1) \tag{5-10}$$

$$Z_2 = R_1 \cdot (1 - jQ_2) \tag{5-11}$$

Sensitivities of Z_2 to C_1 and C_2 are derived respectively as

$$S_{C_1}^{Z_2} = \frac{\partial Z_2}{\partial C_1} \cdot \frac{C_1}{Z_2} = \frac{\omega^2 C_1 C_2 {Z_0}^2}{(1 + j\omega C_1 \cdot Z_0)[1 + j\omega(C_1 + C_2)R_0]} \tag{5-12}$$

$$S_{C_2}^{Z_2} = \frac{\partial Z_2}{\partial C_2} \cdot \frac{C_2}{Z_2} = -\frac{1 + j\omega C_1 \cdot Z_0}{1 + j\omega(C_1 + C_2)R_0} \tag{5-13}$$

The relative variation of Z_2 is given as

$$\frac{dZ_2}{Z_2} = S_{C_1}^{Z_2}\frac{dC_1}{C_1} + S_{C_2}^{Z_2}\frac{dC_2}{C_2} \tag{5-14}$$

Substitution of (5-8)-(5-11) into (5-12) and (5-13) leads to

$$S_{C_1}^{Z_2} = \frac{\partial Z_2}{\partial C_1} \cdot \frac{C_1}{Z_2}\bigg|_{\substack{\text{nominal}\\ \text{values}}} = \frac{Q_1}{j + Q_2} \tag{5-15}$$

$$S_{C_2}^{Z_2} = \frac{\partial Z_2}{\partial C_2} \cdot \frac{C_2}{Z_2}\bigg|_{\substack{\text{nominal}\\ \text{values}}} = \frac{-Q_2}{j + Q_2} \tag{5-16}$$

If the capacitors C_1 and C_2 are ideally matched to each other and lie on the same Q circle, we have

$$dC_1/C_1 = dC_2/C_2 \tag{5-17}$$

$$Q_1 = Q_2 \tag{5-18}$$

Substitution of (5-15)- (5-18) into (5-14) leads to

$$\frac{dZ_2}{Z_2} = S_{C_1}^{Z_2}\frac{dC_1}{C_1} + S_{C_2}^{Z_2}\frac{dC_2}{C_2} = \frac{Q_1 - Q_2}{j + Q_2}\cdot\frac{dC_1}{C_1} = 0 \tag{5-19}$$

From (5-19) it can be seen that Z_2 has a zero sensitivity to capacitance variations if the proposed network satisfies (5-8), (5-9), (5-17) and (5-18). The zero sensitivity comes from the variation cancellation mechanism. When C_1 experiences a positive deviation from the nominal value, its susceptance will be increased. Correspondingly, on the reflection coefficient plane, its transformation trace will be longer. Ideally matched C_2 will experience the same rate of change, resulting in a smaller reactance and a shorter transformation trace on the reflection coefficient plane, which compensates the change caused by C_1 and thus maintains the length of the total transformation traces.

5.2.3 *Process-Variation Insensitive Matching Networks*

The one-step impedance transformation using a single L-section in Figure 5-3 can be broken into two L-sections of the same Q factor to implement the element of PVI network. A two-step impedance matching network with two L-sections of alternating passive components is shown in Figure 5-5.

Application of $1+Q^2$ theory in [5.4] leads to

$$\sqrt{R_2} = (1 + Q_2^2)\cdot\sqrt{R_0} \tag{5-20}$$

$$\omega L_1 = Q_2 \cdot R_0 \tag{5-21}$$

$$\frac{1}{\omega C_1} = \frac{1 + Q_2^2}{Q_2}\cdot R_0 \tag{5-22}$$

$$\frac{1}{\omega C_2} = Q_2\left(1 + Q_2^2\right)\cdot R_0 \tag{5-23}$$

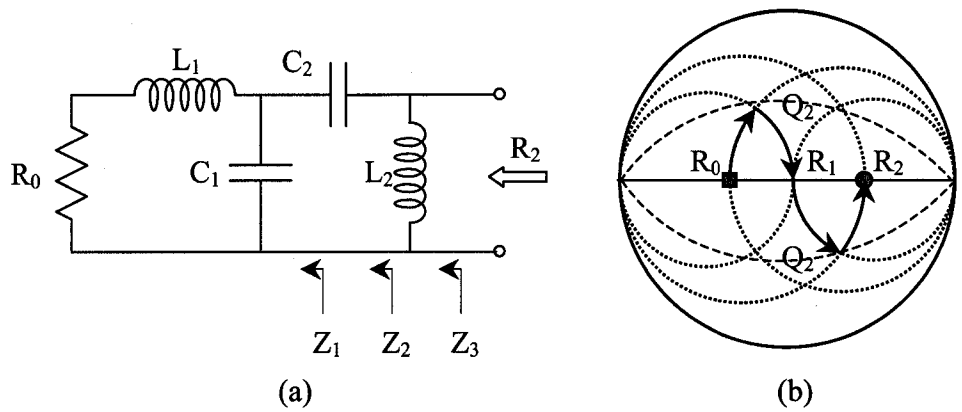


Figure 5-5. (a) A PVI network with two L-sections, (b) transformation traces on Smith Chart.

$$\omega L_2 = \frac{\left(1+Q_2^2\right)^2}{Q_2} \cdot R_0 \tag{5-24}$$

If the capacitors and the inductors are ideally matched to each other respectively, we have

$$\frac{dC_1}{C_1} = \frac{dC_2}{C_2} \tag{5-25}$$

$$\frac{dL_1}{L_1} = \frac{dL_2}{L_2} \tag{5-26}$$

Denote the output impedances of the two-step impedance matching network looking left before and after L_2 in Figure 5-5 respectively as

$$Z_2 = \frac{R_0 + j\omega L_1}{1-\omega^2 L_1 C_1 + j\omega C_1 R_1} + \frac{1}{j\omega C_2} \tag{5-27}$$

$$Z_3 = \frac{j\omega L_2 \cdot Z_2}{Z_2 + j\omega L_2} \tag{5-28}$$

Sensitivities of Z_2 to C_1 and C_2 are derived as

$$S_{C_1}^{Z_2} = \frac{\partial Z_2}{\partial C_1} \cdot \frac{C_1}{Z_2} = \frac{\omega^2 C_1 C_2 \left(R_0 + j\omega L_1\right)^2}{\left(1-\omega^2 C_1 L_1 + j\omega C_1 R_0\right) \cdot A} \tag{5-29}$$

$$S_{C_2}^{Z_2} = \frac{\partial Z_2}{\partial C_2} \cdot \frac{C_2}{Z_2} = -\frac{1-\omega^2 C_1 L_1 + j\omega C_1 R_0}{A} \tag{5-30}$$

Sensitivities of Z_3 to L_1 and L_2 are derived as

$$S_{L_1}^{Z_3} = \frac{\partial Z_3}{\partial L_1} \cdot \frac{L_1}{Z_3} = \frac{\omega^4 C_2^2 L_1 L_2}{A \cdot (A+B)} \tag{5-31}$$

$$S_{L_2}^{Z_3} = \frac{\partial Z_3}{\partial L_2} \cdot \frac{L_2}{Z_3} = \frac{A}{A+B} \tag{5-32}$$

where

$$A \equiv 1-\omega^2 (C_1 + C_2) L_1 + j\omega (C_1 + C_2) R_0 \tag{5-33}$$

$$B \equiv -\omega^2 C_2 L_2 + \omega^4 C_1 C_2 L_1 L_2 - j\omega^3 C_1 C_2 L_2 R_0 \tag{5-34}$$

Denote the summation of $S_{C_1}^{Z_2}$ and $S_{C_2}^{Z_2}$, $S_{L_1}^{Z_3}$ and $S_{L_2}^{Z_3}$ as $S_C^{Z_2}$ and $S_L^{Z_3}$ respectively. Substitution of (5-21)-(5-24) and (5-29)-(5-32) into S_C^{Z2} and S_L^{Z3} leads to

$$S_C^{Z_2} = S_{C_1}^{Z_2} + S_{C_2}^{Z_2} = 0 \Big|_{\substack{\text{nominal} \\ \text{values}}} \tag{5-35}$$

$$S_L^{Z_3} = S_{L_1}^{Z_3} + S_{L_2}^{Z_3} = 0 \Big|_{\substack{\text{nominal} \\ \text{vaules}}} \tag{5-36}$$

The relative variation of Z_3 is obtained as

$$\begin{aligned} \frac{dZ_3}{Z_3} &= S_{C_1}^{Z_3} \frac{dC_1}{C_1} + S_{C_2}^{Z_3} \frac{dC_2}{C_2} + S_{L_1}^{Z_3} \frac{dL_1}{L_1} + S_{L_2}^{Z_3} \frac{dL_2}{L_2} \\ &= \frac{\partial Z_3}{\partial Z_2} \frac{Z_2}{Z_3} \left(\frac{\partial Z_2}{\partial C_1} \frac{dC_1}{Z_2} + \frac{\partial Z_2}{\partial C_2} \frac{dC_2}{Z_2} \right) + S_{L_1}^{Z_3} \frac{dL_1}{L_1} + S_{L_2}^{Z_3} \frac{dL_2}{L_2} \end{aligned} \tag{5-37}$$

Substitution of (5-25), (5-26), (5-29)-(5-32) into (5-37) leads to

$$\frac{dZ_3}{Z_3} = \frac{\partial Z_3}{\partial Z_2} \frac{Z_2}{Z_3} \cdot S_C^{Z_2} \cdot \frac{dC_1}{C_1} + S_L^{Z_2} \cdot \frac{dL_1}{L_1} \Big|_{\substack{\text{ideal} \\ \text{matching}}} = 0 \Big|_{\substack{\text{nominal} \\ \text{values}}} \tag{5-38}$$

Therefore with the condition of ideal matched passive components, Z_3 has a zero deviation to process variation at nominal values because of the cancellation mechanism mentioned before.

By using the 2-step matching in Figure 5-5 instead of 1-step matching shown in Figure 5-3, another immediate advantage is the lowered Q that leads to relaxation on bandwidth.

5.2.4 *Implementation of PVI networks*

The proposed network can be implemented to realize narrowband impedance matching from an arbitrary source impedance to any objective impedance. Denote the source and objective impedances respectively as Z_0 and Z_2, we have

$$Z_0 = R_0 + jX_0 = R_0' \| jX_0' \tag{5-39}$$

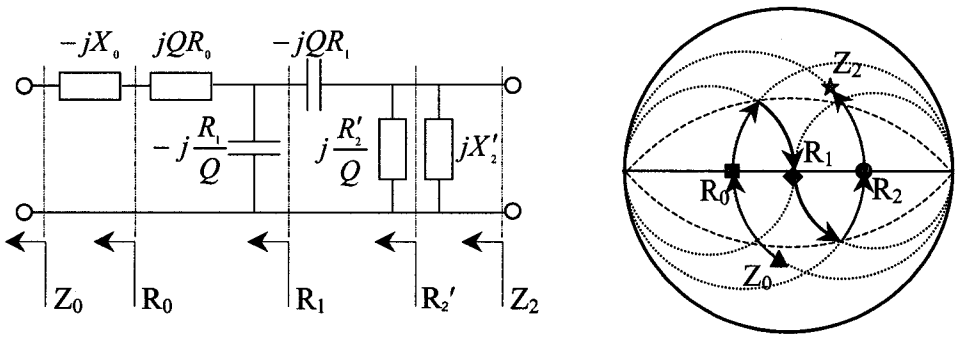
$$Z_2 = R_2 + jX_2 = R_2' \| jX_2' \tag{5-40}$$

If $R_0 < R_2'$, the network in Figure 5-6 can be used to transform R_0+jX_0 to $R_2' \| jX_2'$, where the transformation from R_0 to R_2' is broken into two equal-Q steps to implement the PVI network. Application of $1+Q^2$ theory in [5.4] leads to

$$R_1 = \sqrt{R_0 R_2'} \tag{5-41}$$

$$1+Q^2 = \sqrt{R_2' / R_0} \tag{5-42}$$

The first component can be a capacitor or an inductor, depending on the sign of its reactance of $j \cdot (QR_0 - X_0)$. The second component is a capacitor of which the reactance is equal to $-j \cdot R_1/Q$. The third is a capacitor of which the reactance is equal to $-j \cdot Q R_1$. The fourth can be a capacitor or an inductor, depending on the sign of its reactance of $j R_1'/Q \| jX_2'$.



(a) (b)

Figure 5-6. (a) Realization of the PVI network, (b) illustration of transformation traces on Smith Chart.

If $R_0 \geq R_2'$, then $R_0' \geq R_2$ because $R_0' \geq R_0$ and $R_2' \geq R_2$. The given network can be used to transform R_2+jX_2 to $R_0' \parallel jX_0'$.

5.3 Monte Carlo Simulations of PVI Matching Networks

5.3.1 *Comparison for Ideal Cases*

An example of matching 50 Ω to 100 Ω at a frequency of 5.3 GHz is used to demonstrate the performance improvement from an L-section network to the proposed PVI network. These two involved networks are shown in Figure 5-7 with the passive component values summarized in Table 5-1. The Q factors of these two networks are 1 and 0.644 respectively. The L-section consists of a series inductor and a shunt capacitor. Another configuration with a series capacitor and a shunt inductor can be used but it has similar properties, so only one configuration is included in this example.

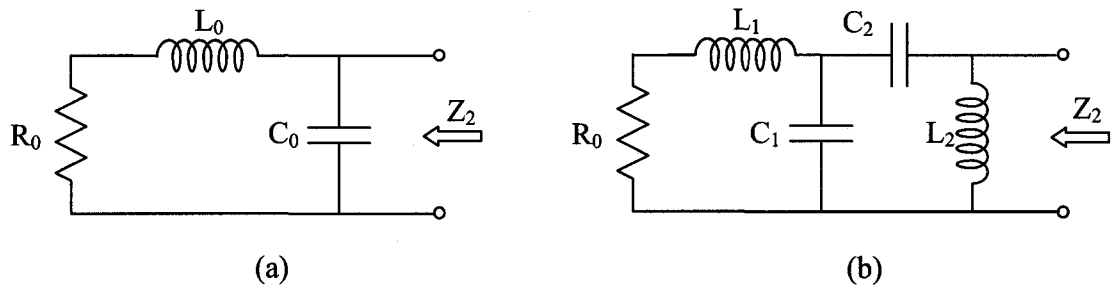


Figure 5-7. Comparison between (a) an L-section network, (b) the PVI network.

Table 5-1. Summary of passive component values used in the matching networks

L-section network			PVI network				
C_0	L_0	Q_0	C_1	L_1	C_2	L_2	Q_1
300.3	1.501	1.00	273.3	0.9663	659.9	4.666	0.644
fF	nH		fF	nH	fF	nH	

The process variations of capacitors and inductors are assumed to be of a Gaussian distribution with a mean (μ) of 0 and a standard deviation (σ) of 0.06 so that virtually all the component variations are within ±20% range of the nominal values. The Gaussian probability density function (PDF) is shown in Figure 5-8. The capacitors and the inductors in the PVI network are assumed to be ideally matched to each other.

The reflection coefficient Γ_2 of the output impedance Z_2 of each network is used as a measure of the impedance transformation. Γ_2 and Γ_2' are evaluated using normalization impedances of 50 Ω and the nominal value of R_2 respectively. The nominal values for Γ_2 and Γ_2' are 0.333 (–9.54 dB) and 0 (-∞ dB) respectively.

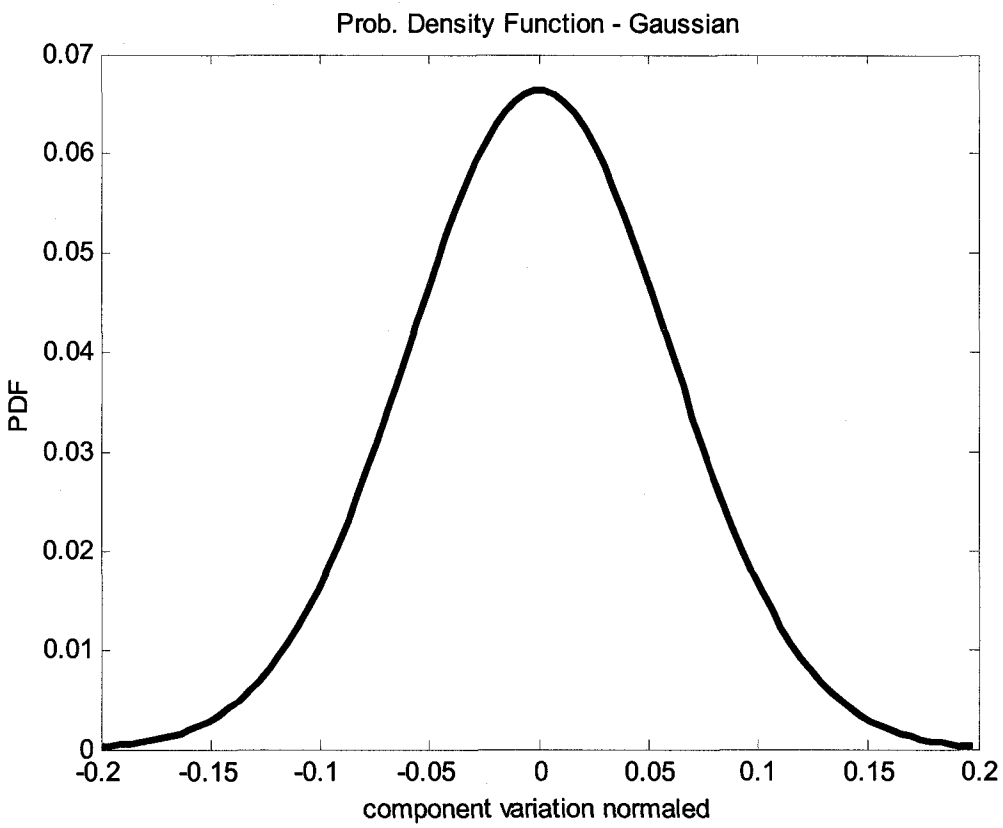


Figure 5-8. Gaussian probability density function of passive component variations.

$$\Gamma_2 = \frac{Z_2 - 50}{Z_2 + 50} \tag{5-43}$$

$$\Gamma_2' = \frac{Z_2 - R_2}{Z_2 + R_2} \tag{5-44}$$

The distributions of Γ_2 for all combinations of variations of capacitors and inductors are plotted in Figure 5-9, where it can be seen that Γ_2 of the L-section network can vary from 0.25-j0.05 to 0.45+j0.14 while Γ_2 of the PVI network is confined into a significantly smaller area. The constant matching circles of $|\Gamma_2'|$ are plotted in Figure 5-9 as well. It can be seen that most of Γ_2' of the L-section fall inside the –15-dB circle while most of Γ_2' of the PVI

network fall inside the –30-dB circle. Therefore the L-section network experiences a significantly larger variation than the PVI network. The probability density function and the cumulative distribution function (CDF) of $|\Gamma_2|$ are plotted in Figure 5-10 and 5-11 respectively.

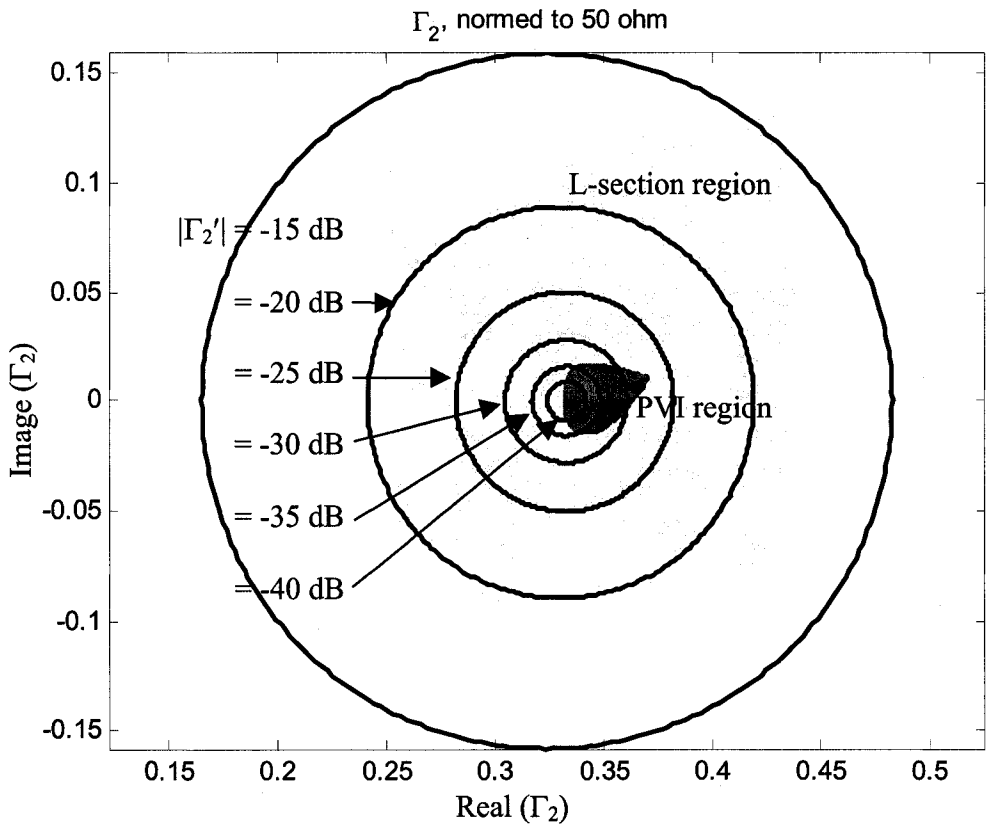


Figure 5-9. Distributions of Γ_2 for the L-section and the PVI network.

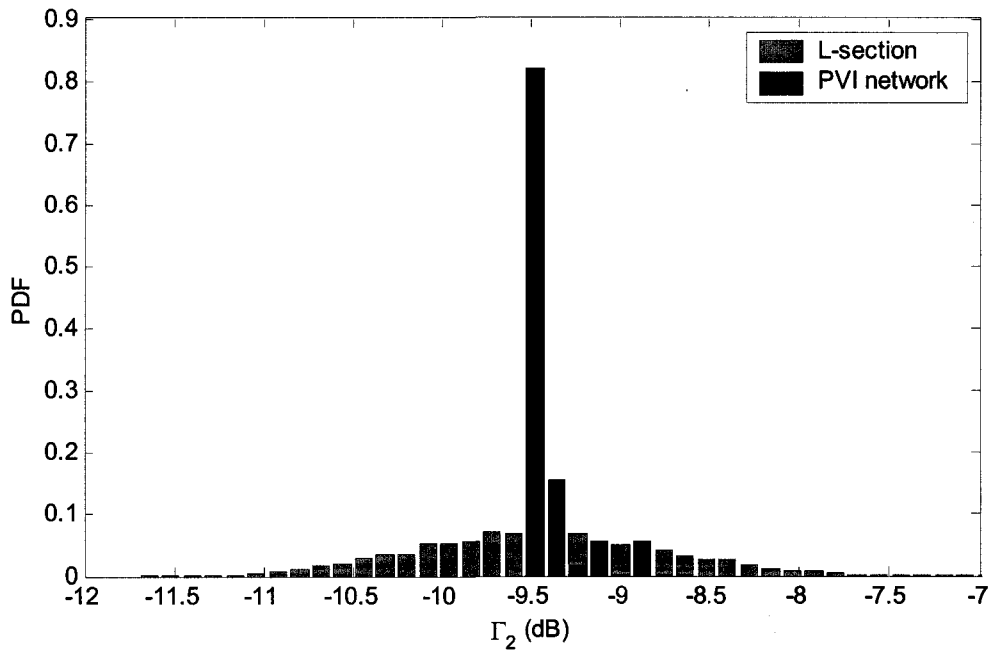


Figure 5-10. Probability density functions of $|\Gamma_2|$ for the L-section and the PVI network.

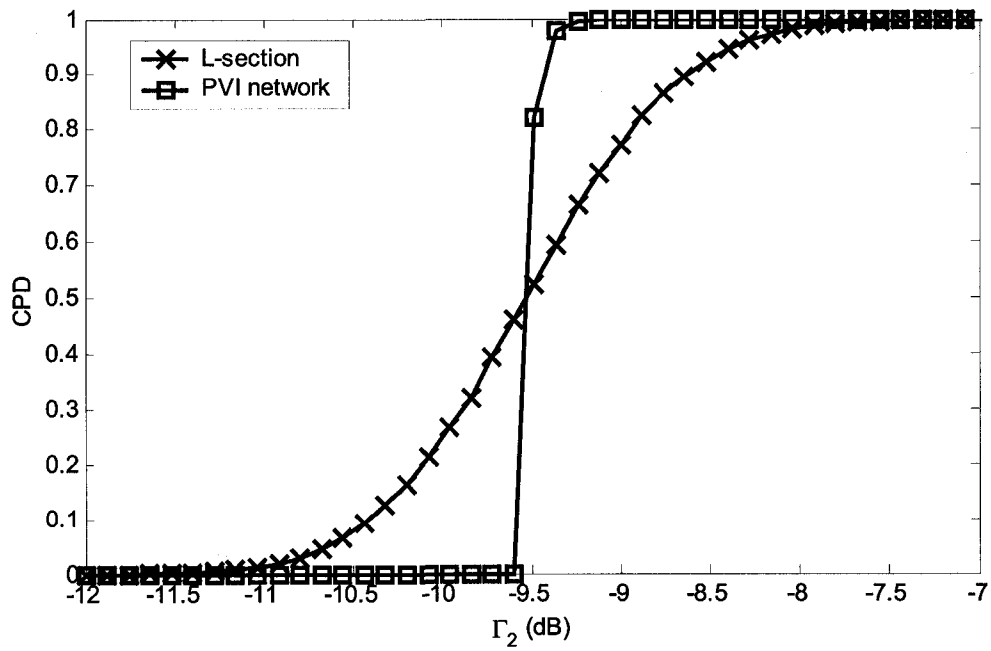


Figure 5-11. Cumulative distributions of $|\Gamma_2|$ for the L-section and the PVI network.

$|\Gamma_2'|$ of different inductor and capacitor variations for the L-section network and the PVI network are plotted in Figure 5-12. The probability density and cumulative distribution functions of $|\Gamma_2'|$ are plotted in Figure 5-13 and 5-14 respectively.

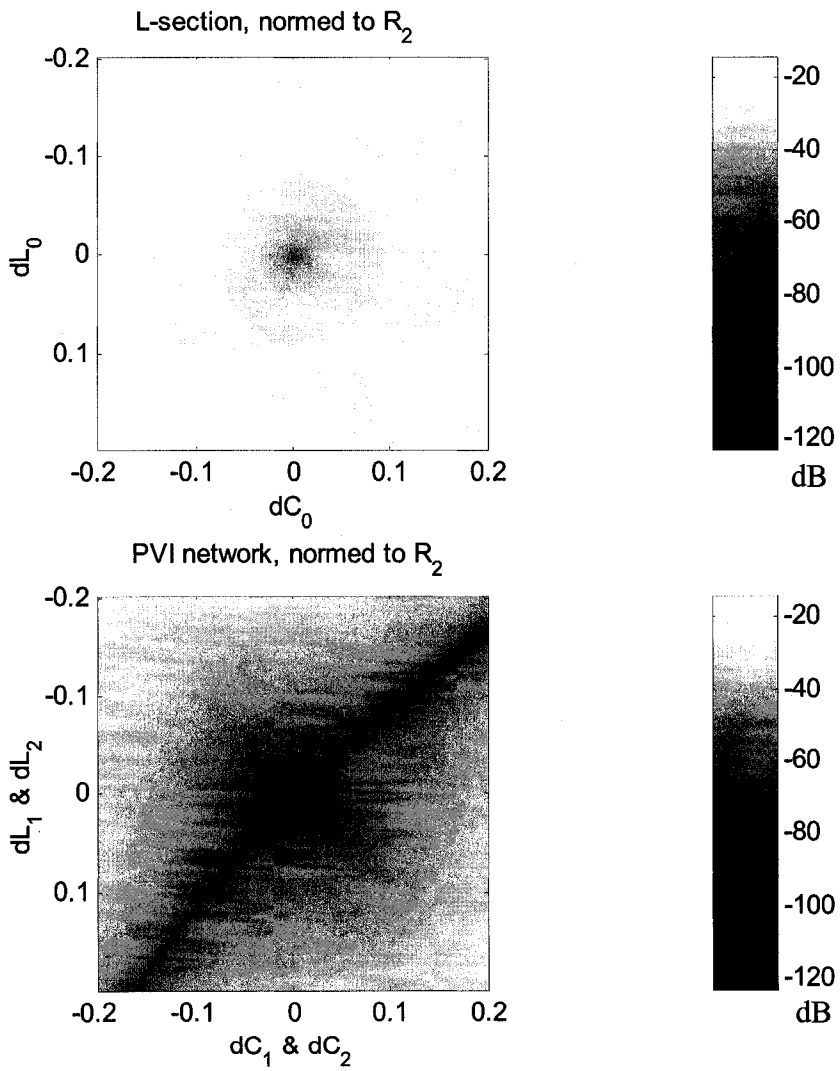


Figure 5-12. $|\Gamma_2'|$ of different inductor and capacitor variations for the L-section and the PVI network.

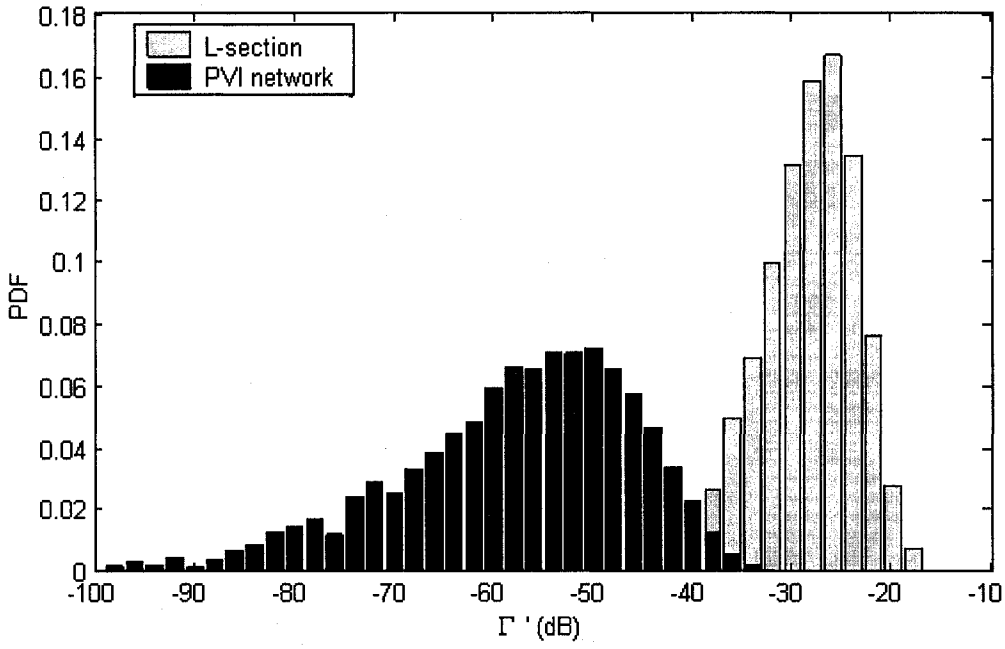


Figure 5-13. Probability density functions of $|\Gamma_2'|$ for the L-section and the PVI network.

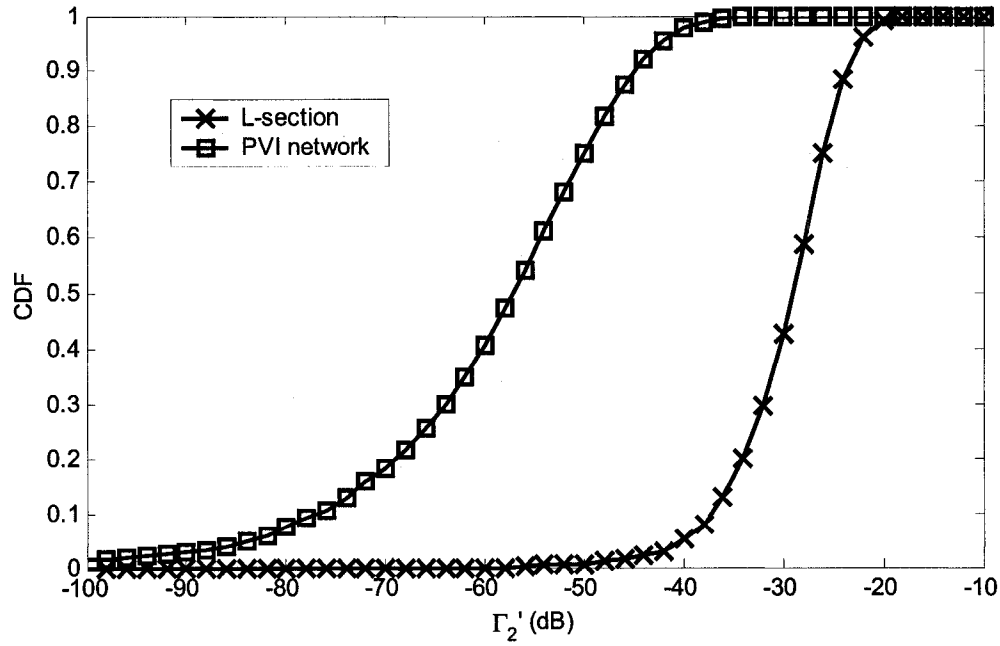


Figure 5-14. Cumulative distribution functions of $|\Gamma_2'|$ for the L-section and the PVI network.

From Figure 5-10 and 5-11, it can be seen that $|\Gamma_2|$ of the L-section spans from –11 dB to –7 dB while $|\Gamma_2|$ of the PVI network is concentrated at the nominal value of –9.5 dB. If the network is used to match 50 Ω to 100 Ω, $|\Gamma_2'|$ can be used to represent the matching level. From Figure 5-12, $|\Gamma_2'|$ of the PVI network is small than that of the L-section for the same inductor and capacitor variations. it can be seen From Figure 5-13 and 5-14, it can be seen that $|\Gamma_2'|$ of the L-section is distributed around –25 dB while $|\Gamma_2'|$ of the PVI network is distributed around –50 dB. Therefore by using the PVI network, the variation of the impedance transformation is confined into a small region thus the matching level can be maintained.

5.3.2 *Monte Carlo Simulations for the real-world cases*

The above case is analyzed under ideal conditions. In reality, when the PVI network is realized in the circuit design, the capacitors and the inductors cannot be ideally matched to each other [5.2]. Mismatch between capacitors does exist though it can be minimized through special layout techniques [5.2]. The integrated on-chip inductors cannot be matched to each other because unlike the capacitors, they cannot be divided into several sub sections since that will increase the capacitance parasitics and result in a lower resonant frequency and other disadvantages. In addition, in order to improve isolation, they cannot be put close to each other.

To incorporate the mismatch between the passive components, the Monte Carlo simulator in circuit design tools is utilized to evaluate the L-section and the PVI network in Figure 5-7. The mismatch between capacitors is assumed to be of Gaussian distribution with a three-sigma figure of 3%. Inductors are considered correlated since they are likely to

experience similar process variation under the same manufacturing condition. The correlation coefficient is assumed to be 0.4.

There are four cases considered in the Monte Carlo simulation as

1) L-section: the one-step L-section network as shown in Figure 5-7(a),

2) PVI worst-case: the PVI network as shown in Figure 5-7(b) with independent passive components,

3) PVI real-case: the PVI network as shown in Figure 5-7(b) with mismatched capacitors and partially correlated inductors,

4) PVI ideal-case: the PVI network as shown in Figure 5-7(b) with ideally matched capacitors and inductors.

The probability density functions of the capacitors and inductors generated in the Monte Carlo simulation are plotted in Figure 5-15. The distributions of Γ_2 and the cumulative distributions of Γ_2' based on ten thousand samples in each case are plotted in Figure 5-17 and Figure 18 respectively. The statistical properties of the PVI networks are compared to that of the L-section network as shown in Table 5-2.

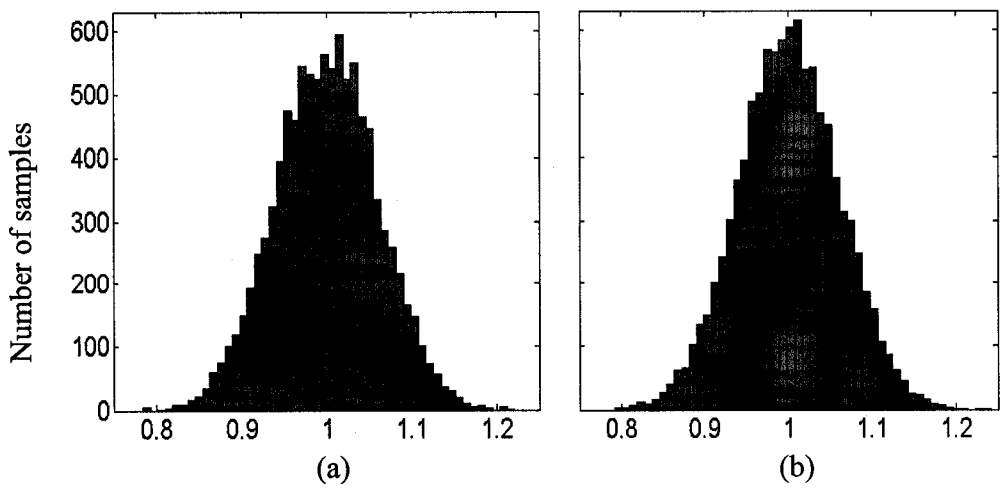


Figure 5-15. Probability density distributions of (a) capacitors, (b) inductors.

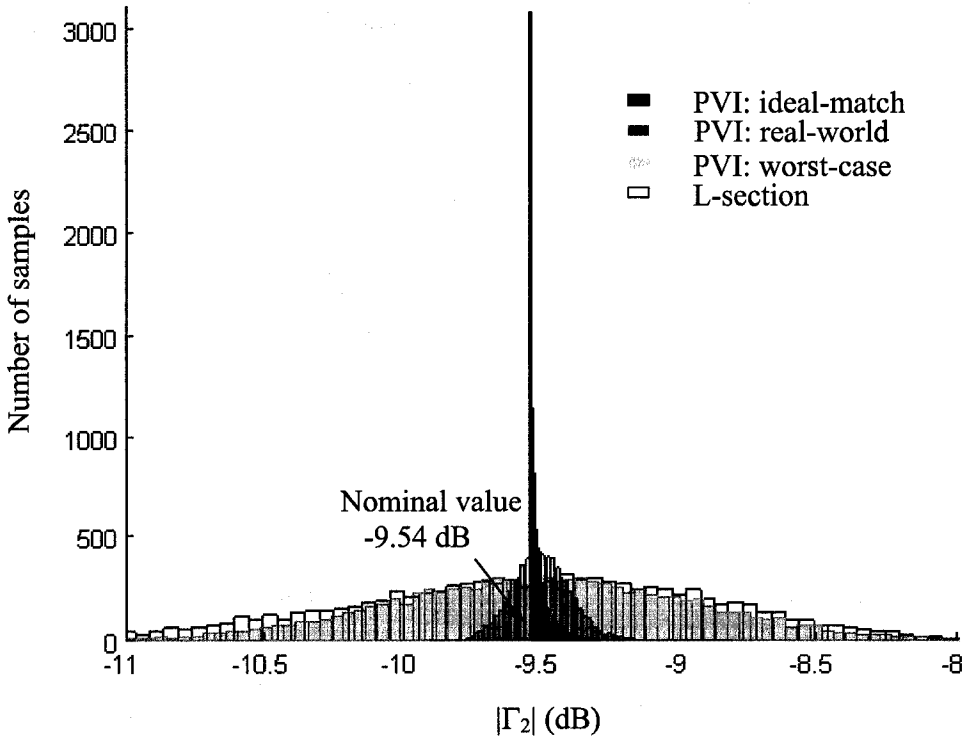


Figure 5-16. PDFs of $|\Gamma_2|$ in Monte Carlo simulations for the L-section and the PVI network.

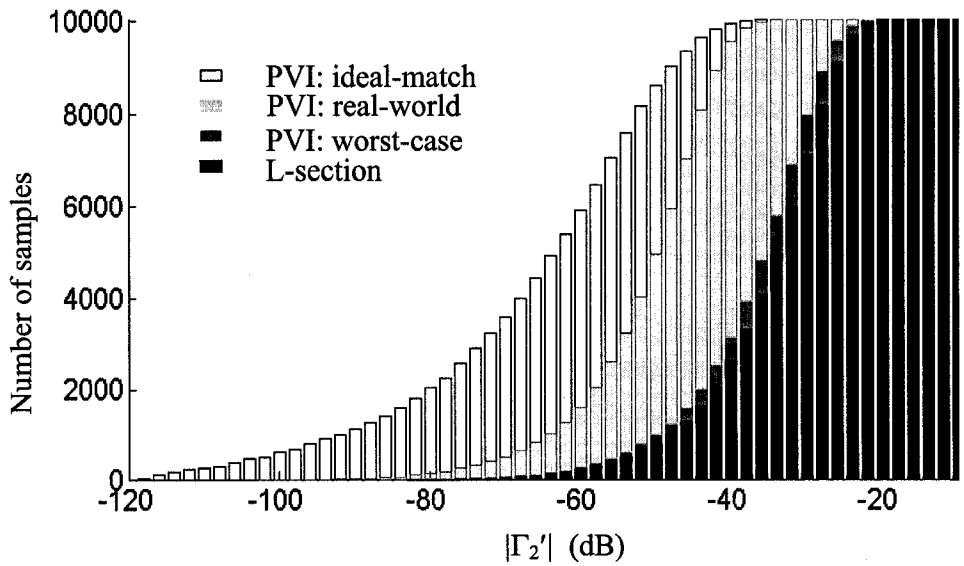


Figure 5-17. CDFs of $|\Gamma_2'|$ in Monte Carlo simulations for the L-section and the PVI network.

Table 5-2. Statistical properties of the PDFs of $|\Gamma_2|$ for the L-section and the PVI network

Statistics	L-section	PVI network		
		Worst-case	Real-case	Ideal-case
μ (dB)	-9.57	-9.51	-9.50	-9.51
σ (dB)	0.697	0.572	0.108	0.049
Min (dB)	-12.5 (81.1 Ω)	-11.7 (85.1 Ω)	-9.91 (97.0 Ω)	-9.54 (100.0 Ω)
Max (dB)	-7.40 (124.4 Ω)	-7.44 (123.8 Ω)	-8.82 (106.8 Ω)	-9.02 (104.8 Ω)
Span (dB)	5.1 (43.3 Ω)	4.3 (38.7 Ω)	1.1 (9.8 Ω)	0.5 (4.8 Ω)

Table 5-3. Cumulative distributions of $|\Gamma_2'|$ for the L-section and the PVI network

$\|\Gamma_3'\|$	L-section	PVI network		
		Worst-case	Real-case	Ideal-case
-80 dB	0.2%	0.3%	1.6%	20.5%
-70 dB	0.7%	0.8%	5.1%	35.7%
-60 dB	2.5%	2.8%	16.2%	59.0%
-50 dB	8.0%	10.0%	49.4%	85.9%
-40 dB	26.4%	31.3%	95.3%	98.9%
-30 dB	71.0%	79.6%	100.0%	100.0%
-20 dB	99.9%	100.0%	100.0%	100.0%
-10 dB	100.0%	100.0%	100.0%	100.0%

From Figure 5-16 and Table 5-2, it can be seen that in the PVI ideal case, Γ_2 is concentrated around the nominal value with a very small spread of 0.049 dB. Correspondingly, the impedance variation span is 4.8 Ω for component variations up to ±20%. In the PVI real case, Γ_2 is still centered around the nominal value but with a spread

two times larger and correspondingly an impedance variation span of 9.8 Ω, while in the PVI worst case and the L-section case, Γ_2 suffers from a significantly larger spread with impedance variation spans of 38.7 Ω and 43.3 Ω respectively. The passive components in the PVI worst case in the Monte Carlo simulation are very weakly correlated to each other, contributing to a slight better performance than that of the L-section.

From Figure 5-17 and Table 5-3, it can be seen that in both the PVI ideal and real cases, over 95% of the samples are matched better than –40 dB, equivalently within ±2% range of the desired value R_2. Only 26.4% of the samples in the L-section case and 31.3% in the PVI worst case reach to –40-dB matching level.

From the simulation results it can be concluded that the proposed PVI matching network with matched components can lead to a significant improvement in immunity from process variation for on-chip impedance matching.

A further Monte Carlo simulation reveals how the matching ratio between passive components affects the performance of the PVI network. In this Monte Carlo simulation, the capacitors are assumed to be independent, mismatched and matched respectively. The inductors are assumed to be independent, correlated and matched respectively. The mismatch ratio and the correlation coefficient remain the same. Thus, there are in total nine different cases for the PVI network, which is summarized in Table 5-4. The L-section case is considered as case 1 in Table 5-4.

The mean values and the standard deviations of these ten distributions are summarized in Table 5-5. The standard deviations are plotted in Figure 5-18. The distribution of Γ_2 for the

L-section is plotted in Figure 5-19. The distributions of Γ_2 for all nine combinations are plotted in Figure 5-20.

From the simulation data, it can be observed that the means of $|\Gamma_2|$ for all ten cases are close to the nominal value of –9.5 dB. Therefore, a smaller standard deviation represents a better performance of impedance matching under process variation.

It can be seen that the L-section case 1, with the largest standard deviation, has the worst performance, while the performance of cases 2 to 10 is primarily dependent on capacitor matching properties. Matched-capacitor cases 8-10, with the smallest standard deviations, have the best performance. Mismatched-capacitor cases 5-7, with medium standard deviations, have fair performance. Independent-capacitor cases 2-4 are among the worst. Capacitor matching ratio dominates the performance while the inductors play a minor role. Therefore, a PVI network with precision matching capacitors will significantly improve the immunity of impedance matching to process variation.

Table 5-4. Case numbers of all combinations of variations

Capacitor / Inductor	PVI network		
	Independent	Mismatched	Matched
Independent	2	5	8
Correlated	3	6	9
Matched	4	7	10
L-section	1		

Table 5-5. Mean values (μ) and standard deviations (σ) of all ten cases

Cases	1	2	3	4	5	6	7	8	9	10
μ (dB)	-9.558	-9.502	-9.506	-9.513	-9.498	-9.500	-9.510	-9.496	-9.501	-9.508
σ (dB)	0.697	0.591	0.581	0.576	0.115	0.108	0.101	0.056	0.051	0.050

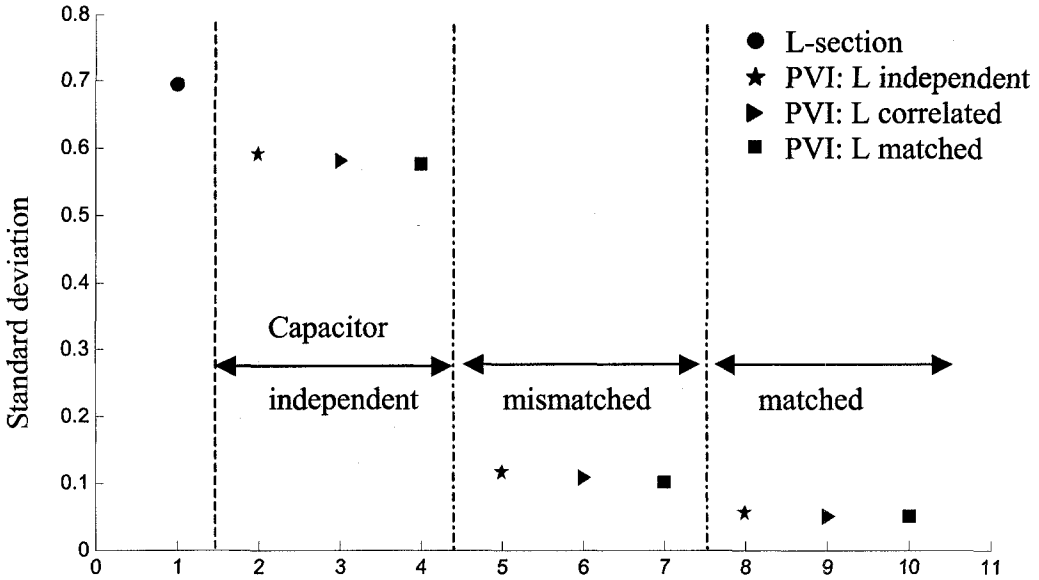


Figure 5-18. Standard deviations of $|\Gamma_2|$ for the simulated ten cases.

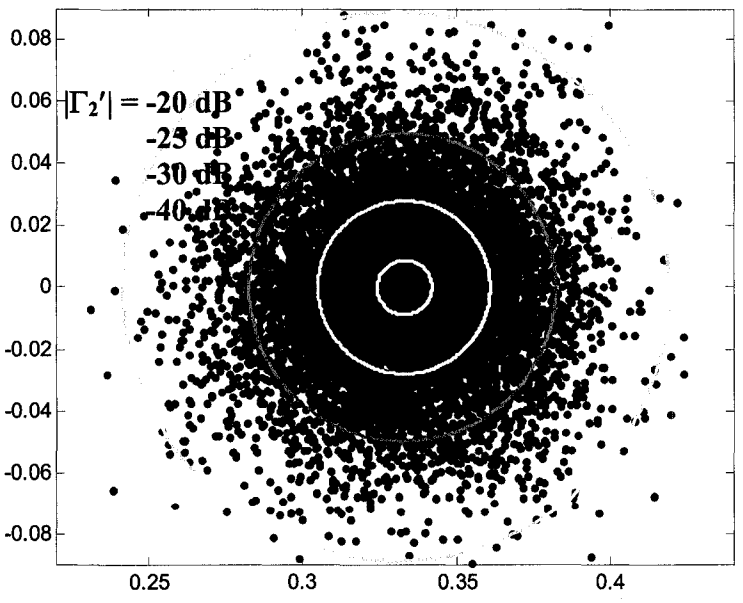


Figure 5-19. Distributions of Γ_2 for the L-section.

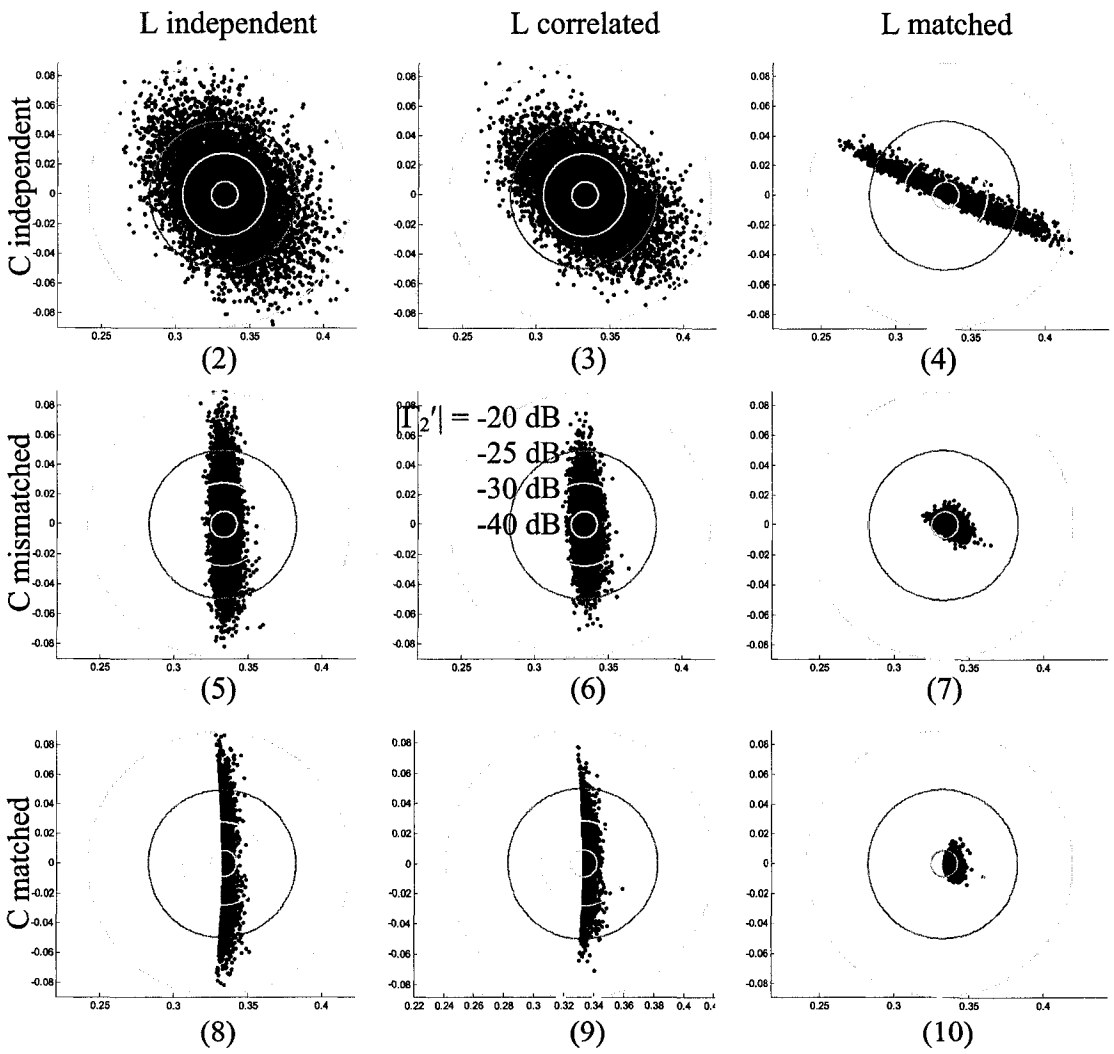


Figure 5-20. Distributions of Γ_2 of all nine combinations of variations for the PVI network.

5.4 Conclusions

In this chapter, a PVI impedance matching network is proposed and verified in simulation. This structure significantly improves the circuit immunity to process variation.

The PVI network utilizes precision matching capacitors. Therefore, the layout design is critical to realize the process-variation independence. Matching between capacitors and inductors should be carefully examined.

The structure will involve more passive components and thus consume more area. In addition, by switching from one-step matching to two-step matching, the inductance, if used in shunt, will have a high value, which leads to higher requirement, i.e. higher Q, for the on-chip inductors. However, enhancement in the yield will likely compensate for these limitations.

References:

[5.1] P. L. D. Abrie, *The Design of Impedance-Matching Networks for Radio-Frqeuency and Microwave Amplifiers*, Norwood, MA: Artech House Inc., 1985.

[5.2] A. Hastings, *The Art of Analog Layout, New Jersey*, Englewood Cliffs, Jew Jersey: Prentice-Hall Inc., 2001.

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[5.5] G. D. Vendelin, A. M. Pavio, U. L. Rohde, *Microwave Circuit Design Using Linear and Nonlinear Techniques*, New York: J. Wiley & Sons, 1990.

CHAPTER 6 . CONCLUSIONS

6.1 Summary

In Chapter 3 a multi-port noise analysis approach based on the well-known two-port noise theory is presented to explore the noise behavior of MOSFETs. An explicit formulation is given for a three-port-to-two-port noise transformation to anticipate how the source degeneration inductor changes the two-port noise parameters. This approach is applied in the design of a 5.3-GHz CMOS LNA to achieve a simultaneous noise and gain match. Theoretical implementation of the circuit gives a 1.02-dB NF and a 17.1-dB gain with the circuit drawing 4.2 mA from a 1.5-V power supply.

In chapter 4, a new design approach on optimization of the impedance matching of an LNA is presented. This approach considers both input and output impedance matching to achieve a high gain performance. Using this approach and the multi-port noise analysis, the feedback of the 5.3-GHz LNA is optimized and the circuit is implemented in a CMOS 0.18-μm process. The measurement gives a gain of 5.2 dB at 5.3 GHz. The maximum measured gain is 7.2 dB. The nominal input and output impedance matching levels are –9.3 dB and –8.9 dB respectively. The nominal isolation is –42.8 dB. The noise figure is estimated to be 4.8 dB from the updated simulation.

From measurement data it is observed that the impedance matching is shifted to a lower frequency due to the variations of the passive components in the matching network. A PVI network is proposed to better tolerate the process variation. The PVI network utilizes the idea of precision matching to achieve a cancellation of variation. Sensitivity analysis reveals its

high immunity to process variation. The improvement from a regular L-section network to the PVI network is demonstrated in Monte Carlo simulations.

6.2 Conclusions

The presented theoretical analysis and design methodologies contribute to different areas in the field of RF IC design.

It is demonstrated in Chapter 3 that a three-port approach is necessary to fully characterize a three-terminal MOSFET. Three-port S parameters are needed to model the linear features of a MOSFET when all of its three terminals are not grounded. A three-port noise matrix is needed to characterize the noise behavior of a MOSFET accordingly.

By means of multi-port noise analysis, the feedback effect on the two-port noise parameters can be analyzed accurately. The multi-port noise analysis also provides a method to study the effect of multiple feedback on noise performance.

The procedure of how to extract a multi-port noise matrix from two-port noise simulation suggests a way to incorporate multi-port noise simulation in current circuit simulation tools so that multi-port analysis can be supported.

The optimization technique discussed in Chapter 4 provides an analytical solution to design an LNA to meet multiple design goals of noise, gain, and impedance matching. This technique considers simultaneously multiple goals in tuning feedback to achieve an optimum solution. Since only S and noise parameters are needed, it is a generic approach that can be applied to many other semiconductor technologies.

The novel PVI network proposed in Chapter 5 utilizes a simple structure to achieve on-chip impedance matching that tolerates process variation. While currently impedance

matching of many applications is realized using external matching networks, this technique provides a suitable solution for higher level of integration by eliminating external matching networks. More passive components are used. Therefore, the die area is increased. However, the board area is reduced.

6.3 Recommendations for Future Work

There are various challenging issues that need to be addressed in future research. Current noise characterization of MOSFETs in testing is generally a two-port approach. As suggested in Chapter 3, a multi-port noise matrix is necessary to fully characterize a multi-port network. Three-port noise characterization is suggested to improve the noise modeling of a MOSFET or other three-terminal active devices.

The performance of a PVI network relies largely on the capacitor matching ratio. High precision matching capacitors are recommended. Further studies can be carried out on how to realize highly matched capacitors in high frequency domain. Inductors of high Q factor are important to maintain matching performance because on-chip inductors usually have many parasitic components, which will degrade the immunity of a PVI network. Theoretical analysis can be extended to study the effect of parasitics on sensitivities of the PVI network.